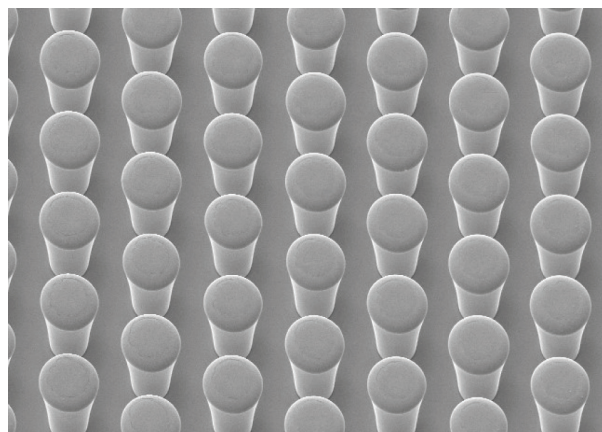




High-rate Copper Pillar Plating Using the Solstice CopperMax Reactor

Modern semiconductor copper plating chemistries include expensive, highly-engineered organic additives that serve to enhance the quality of the plating. However, these additives are readily destroyed when they come in contact with the copper anode of the plating system. This necessitates ongoing replenishment of additives and significantly increases process costs.

However, the proprietary Solstice® CopperMax™ reactor integrates a cationic exchange membrane that separates organic additives from the anode while still allowing high-speed copper cation movement to the wafer. This enables higher plating rates while routinely reducing the user's chemistry costs by more than 95% – and also delivering world-class plated feature uniformity.



High-uniformity copper pillar plating from the Solstice CopperMax reactor

Example Applications

- Wafer level packaging
- Flip-chip interconnects
- Solder bumping (with nickel & solder plating)
- C4 bump
- Thermo-compression bonding
- And more...

Features

- Cation exchange membrane to reduce additive use
- Continuously filtered chemistry, optional carbon filtration
- High-precision wafer rotation
- Adjustable diffuser
- Dry-contact low-maintenance plating rotor
- Customized seal reach
- Levitronix pump with LeviFlow™

Benefits

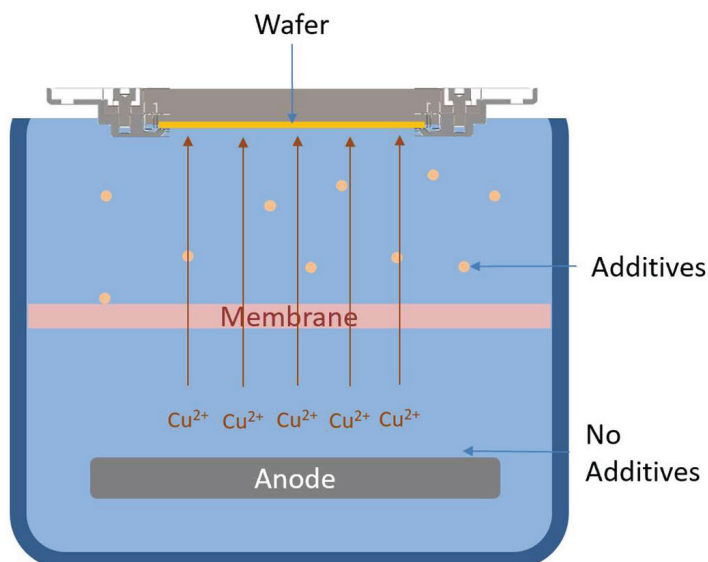
- Additive costs reduced >95%
- Maximized bath life
- Extremely uniform field profile
- Seal reach aligns to existing integration
- Continuously cleaner chemistry
- Precise, consistent flow rate control

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Eliminating additive breakdown

The proprietary design of the Solstice® CopperMax™ reactor dramatically reduces the deterioration of organic additives by using a cationic exchange membrane to keep additives from contacting the anode. This significantly reduces chemistry costs while enhancing copper plating quality.

In other reactors, the plating behavior shifts rapidly as additives break down. The bath metrology begins to return inaccurate readings, which leads to erroneous dosing.



Technical Data

■ Wafer Sizes	75-200 mm	Configurable to non-standard sizes, e.g., 160 mm
■ Wafer Thickness	150µm to >6mm	
■ Wafer Materials	Silicon GaAs GaN on Si, GaN on Sapphire Sapphire Transparent substrates and more	
■ Flow Rate	25 lpm	
■ Plating Rate	>3 µm/min, up to 6.5 µm/min	
■ Within-Wafer Uniformity	<3% (range / 2*mean)	
■ Wafer-to-Wafer Uniformity	<1% (mean-to-mean)	
■ Coplanarity	<5%	

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