

Fundamentals of Electrochemical Deposition

Introduction

Numerous products are manufactured using well-established semiconductor production applications. Electrochemical deposition, i.e., plating, is a well characterized and flexible method for metallization of almost any metal in a wide variety of deposition modes. Additionally, electrochemical deposition offers high productivity, tight process control, and low operating costs.

This document serves to provide background fundamentals of electrochemical deposition in the semiconductor industry for engineers, technicians and other personnel.

General Electrochemical Cell

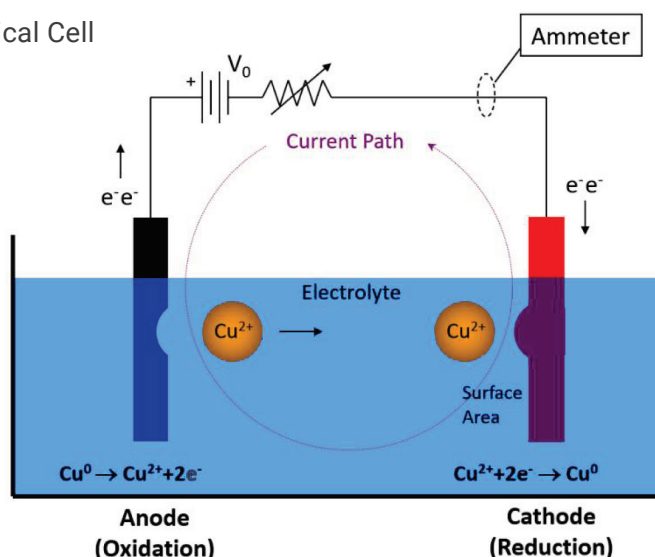
Figure 1 depicts a general electrochemical cell wherein two electrodes are electrically connected to a power supply and submerged together in a metal salt electrolyte. When potential is applied to this closed cell, electrons will flow from anode to cathode. Metal ions are driven to the cathode where electrochemical deposition of the metal occurs.

In the specific case used in the illustration, a copper anode is consumed by the reaction; copper metal is oxidized at the anode surface, replenishing copper ions depleted from the

electrolyte solution via reduction (and thus deposition) at the cathode surface.

Quality plating of metal requires operation of the cell in an “electron-poor” condition. This means that at the surface of the cathode the availability of cations (positively charged metal ions) greatly dominate the availability of electrons. The result is that adjustment of the current density up or down at the cathode surface directly modulates the rate of deposition up or down accordingly.

Figure 1. General Electrochemical Cell



Electrochemical Cell In Semiconductor Wafer Applications

While there are multiple types of plating cells in use in the semiconductor industry, the specifications for leading products and devices drives the use of single-wafer fountain plating. All the major semiconductor device manufacturers use some version of a face down, single wafer, fountain plating reactor. ClassOne Technology's Gen4 Reactor serves as the example plating reactor in this document.

Figure 2 illustrates how the Gen4 reactor replicates the general electrochemical cell for the sake of uniform and repeatable plating of semiconductor wafers.

Present in the Gen4 Reactor are the anode, electrolyte and cathode. The wafer, as the target for metal deposition, serves as the cathode in the cell.

When the plating process is set up properly, the rate of plated metal deposition is directly controlled by the current applied to the reactor. Stated differently, proper electroplating takes place in an "electron-poor" condition. The electrons provided to the system act as a "limiting reagent." Thus, a lower current results in fewer electrons provided to the system over a specific period of time, which results in a slower deposition rate. The current delivered to the reactor is consumed with 98-100% efficiency in the deposition of metal, under normal operating conditions and dependent upon the electrolyte composition.

To be clear, here we are talking about a rate of deposited mass. Most often, the process criteria are defined around a total plated thickness. This simply means we are confining mass (or volume) of plated material to a known area. This is area is called Open Area. For wafers with no photoresist or other insulative mask pattern, this Open Area is 100%. In cases where a photoresist or similar mask is present, Open Area is defined as the percentage of the wafer area where the patterning has exposed the seed metal.

This then means that the driver for plating rate, in terms of plated thickness, is driven by current density, expressed by the variable J , most often in units of amps per square decimeter (ASD) or milliamps per square cm. Current density is thus defined as the quotient of current / open area (Fig. 3).

Figure 3. Plating rate

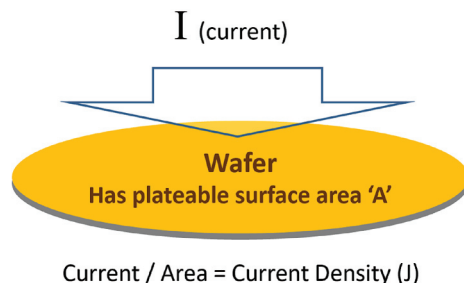
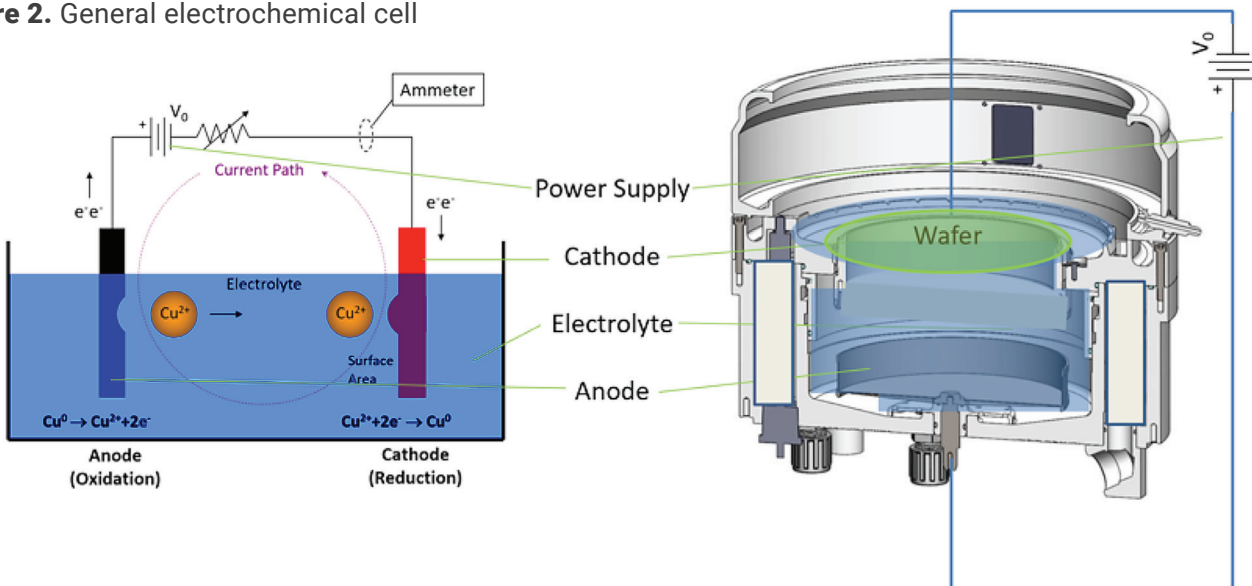


Figure 2. General electrochemical cell



Limiting Current Density

Ohm's Law [1] is, of course, one of the most important formulas defining how electric cells behave, and it is perfectly applicable to the electrochemical deposition cell.

[1] $I = V/R$

where I = Current
 V = Voltage
 R = Resistance

While Ohm's Law accurately represents the relationship between voltage and current in an electrochemical cell, the availability of reactants in the system means that the relationship is not linear for all applied potentials.

Earlier in this document, we explained that quality metal deposition is achieved by operating the cell in an "electron-poor" condition. This condition can be referred to as Charge Control condition (Fig. 4). Thus, as stated, the reaction moves at a rate dictated by the availability of electrons, i.e., current density.

As current density is increased, the availability of electrons draws nearer to the availability of cations at the wafer surface and the conditions migrate into the "mixed region" and possibly into "Mass Transfer Control". In the region of Mass Transfer Control, electrons are no longer a limiting reagent and instead reaction rates are driven by availability of reactants from the bulk electrolyte, for example cations. Thus, the reactions taking place become impeded by depletion of cations which must move across the diffusion layer in order to react.

Meanwhile the electrons will be consumed in a reaction, whether or not there are sufficient cations available to keep up. This means side reactions begin to occur, the specifics of which depend somewhat on the application; but in any case, gas is evolved and typically the concentration of a number of components in the bath begins to shift. Additionally, the deposit on the wafer is of extremely poor quality and results in a wafer-scrap/rework event. Fortunately, plating is a stable process with straightforward control schemes so a quality plating tool using proper operating procedures should never experience such a condition.

The current density at which such unfavorable reactions take place is referred to as the "Limiting Current Density" or LCD and a properly controlled plating process should never approach this condition.

The point at which LCD is reached is dependent on several factors. In other words, it is possible to maneuver LCD to a higher or lower current density by adjusting various parameters. As shown in Figure 5, increasing electrolyte temperature and/or agitation of the fluid at the wafer surface can increase the current density at which LCD is reached. Temperature increases the kinetics of the plating reaction(s). Agitation thins the diffusion layer, thereby increasing the replenishment rate of cations at the surface of the diffusion layer. Likewise, increasing the concentration of cations in the bulk solution can increase availability of cations at the diffusion layer. In all cases, the adjustments have maneuvered the process back to an electron-poor condition, moving the cell back into charge control region.

Figure 4. Voltage-current density relationship

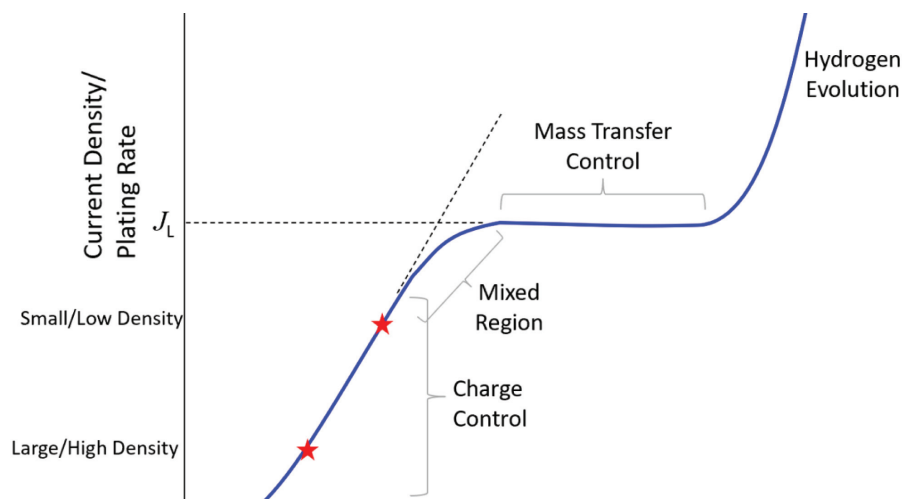
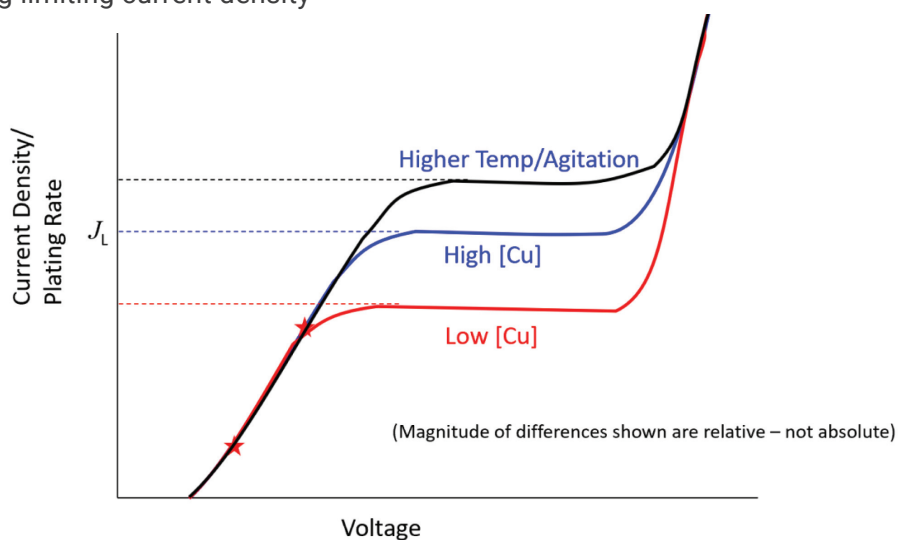


Figure 5. Varying limiting current density

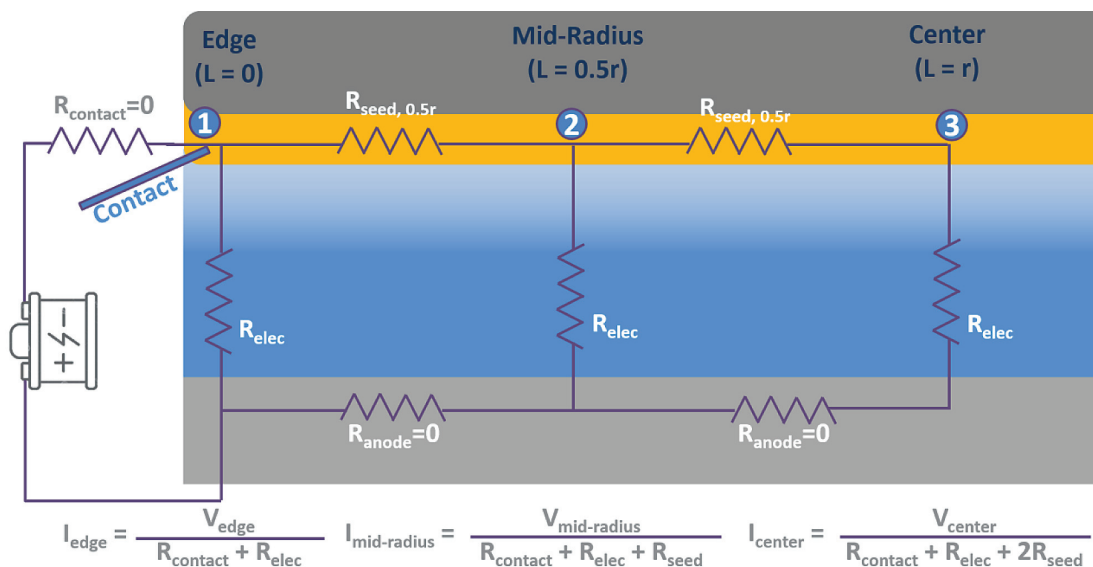
Key factors for Uniform Deposition

Semiconductor plating applications are subject to a number of performance requirements, chief among which is the uniformity of the deposited film. This can be expressed in a number of ways depending on the specific application; but, in short, the film or features should be essentially the same thickness or height everywhere on the wafer.

The key factors driving uniformity are the current density distribution and the uniformity of the diffusion layer. Generally speaking, if the current density is the same everywhere on the wafer, and also well below LCD, then plated film thick-

ness will be the same everywhere on the wafer (assuming no abnormalities are present such as contamination from upstream processes, etc.).

Regarding the diffusion layer, if no significant difference exists in its thickness across the wafer, then cations, which are subject to constant mass transfer rates, cross the diffusion layer in the same amount of time and therefore support uniform plating rates. The diffusion rates of cations will be a non-factor when operating at very low current density. However, when a high plating rate is wanted, mass transport

Figure 6. Current distribution through wafer

becomes a more significant consideration for uniform deposition. This is especially true for cations with low diffusion rates, as this document later addresses.

Based on this understanding, we can confidently say that by defining the correct electric field profile and the correct fluid flow profile, a uniform plated film will be deposited.

Key Factor: Uniform Electric Field

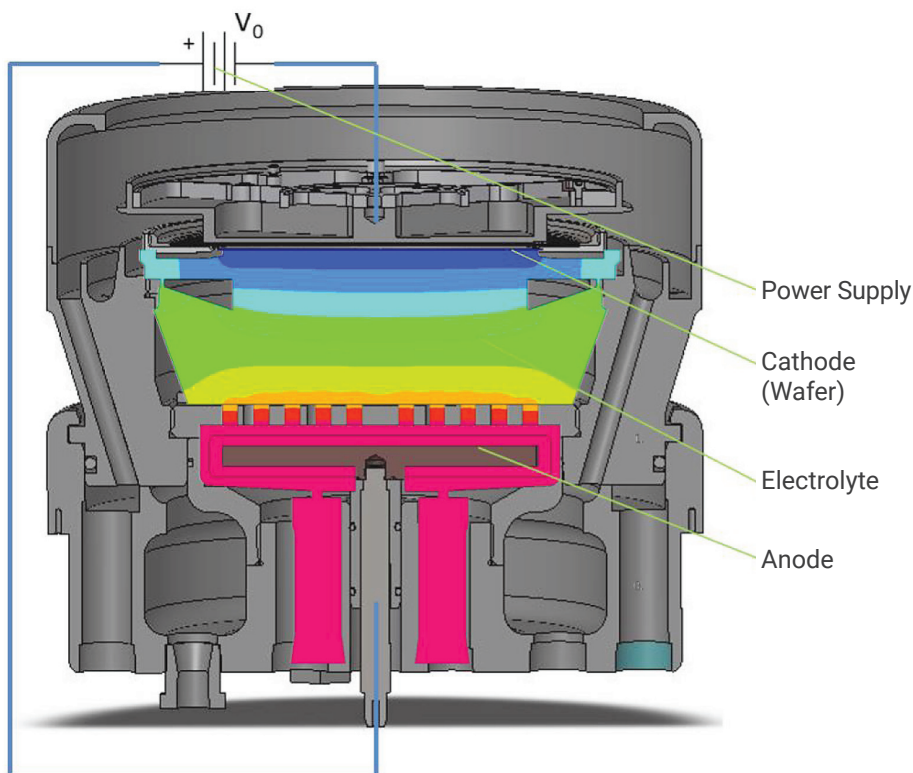
We will start with a description around the electric field profile. Figure 6 depicts a portion of a wafer submerged into a plating electrolyte in preparation to perform plating on it. The full electrochemical cell is depicted including the contact points where the cell electrically connects to the seed layer of the wafer.

The seed layer is necessary to carry the electric current to all areas of the wafer. As seen in the image, the wafer is depicted in three meaningful regions: the wafer edge (where the cell makes electrical contact between the power supply and the wafer), the mid radius, and the center of the wafer.

As we've previously discussed, Ohm's Law applies to electrochemical cells and accordingly the current density incurred at each indicated point on the wafer, which must be the same as each other in support of uniform plating, are dependent on the voltage and resistance particular to each location. As the image shows, the edge of the wafer is much closer to the electrical contacts than the mid radius and much closer than the center. Therefore, it is true that the edge of the wafer will experience a resistance through the seed that is lower than the resistance at mid radius, which in turn is lower than the resistance at wafer center. This is because the current will need to pass through the seed across a distance moving from edge to center.

However, in application, we find that the actual difference in resistance is very low and in fact negligible because the typical seed layer is sufficiently thick that its sheet resistance is well within the "bulk sheet resistance" regime. This means

Figure 7. Electric field profile in Solstice plating reactor (CFD Model)



that, to produce an electric field profile conducive to uniform current density across the wafer, it is necessary to produce the same voltage at all points across the wafer. In other words, the field profile produced by the reactor should have a uniform potential across the entire diameter of the reactor.

Figure 7 depicts an early version of ClassOne's plating reactor with a model of the electric field superimposed over it. The model was created by computational fluid dynamic modeling and is highly accurate in describing the actual field imposed by the reactor. In the picture, one can easily see that no color variation exists at the location of the wafer being plated, meaning that the voltage is the same at every location on the wafer and thus a uniform current density will be achieved.

There is a complication to overcome, and it arises from the fact that the wafer being plated has a terminus, a place where the conductive wafer surface terminates. This may be an insulative seal (as in the case of the ClassOne plating rotor) or if no seal is present, the terminus becomes the edge of the wafer. In both cases, the terminus imposes an abrupt

disruption to the electric field out at the very edge of the wafer. When such a disruption is present in an electric field, the field lines curve away from the insulator and become crowded (Fig. 8).

This crowding of field lines represents actual crowding of the current, thus the edge of the wafer experiences elevated current density and therefore faster plating rates (Fig. 9). If not accounted for, the result will be a wafer plated uniformly across its center with a ring of much thicker metal around the edge.

All plating systems are subject to such current crowding and must employ a means of reducing the current crowding. The most typical means is to include a shield in the reactor. Figure 10 shows the previous illustration but now with a shield added. As compared to the field lines shown in Figure 9, the shield in Figure 10 basically forces the field line crowding further in before the field reaches the wafer surface. Thus, above the shield, the field spreads back out again, resulting in a reduced density of the current and eliminating the region of faster plating.

Figure 8. Example of field line crowding around insulator

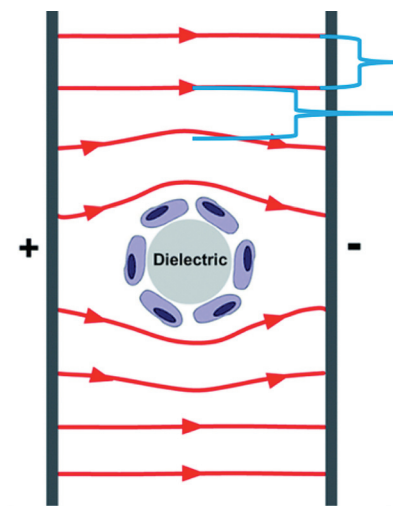


Image citation: Title: "What happens to any insulator when it is placed in any external electric field?" Author: BLAZE (<https://physics.stackexchange.com/users/57983/blaze>), Publication: Physics Stack Exchange. Note: URL: <https://physics.stackexchange.com/q/348458> (version: 2017-08-09),

Figure 9. Current crowding at plating seal – with no shield

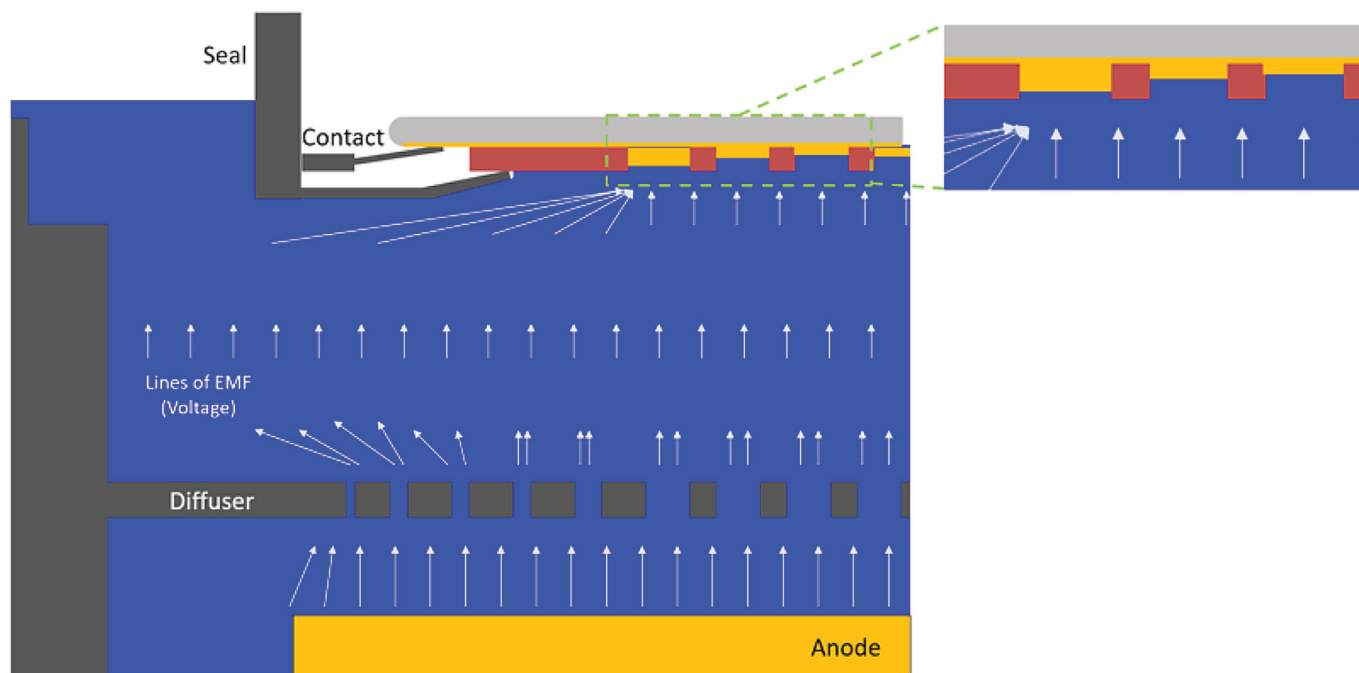
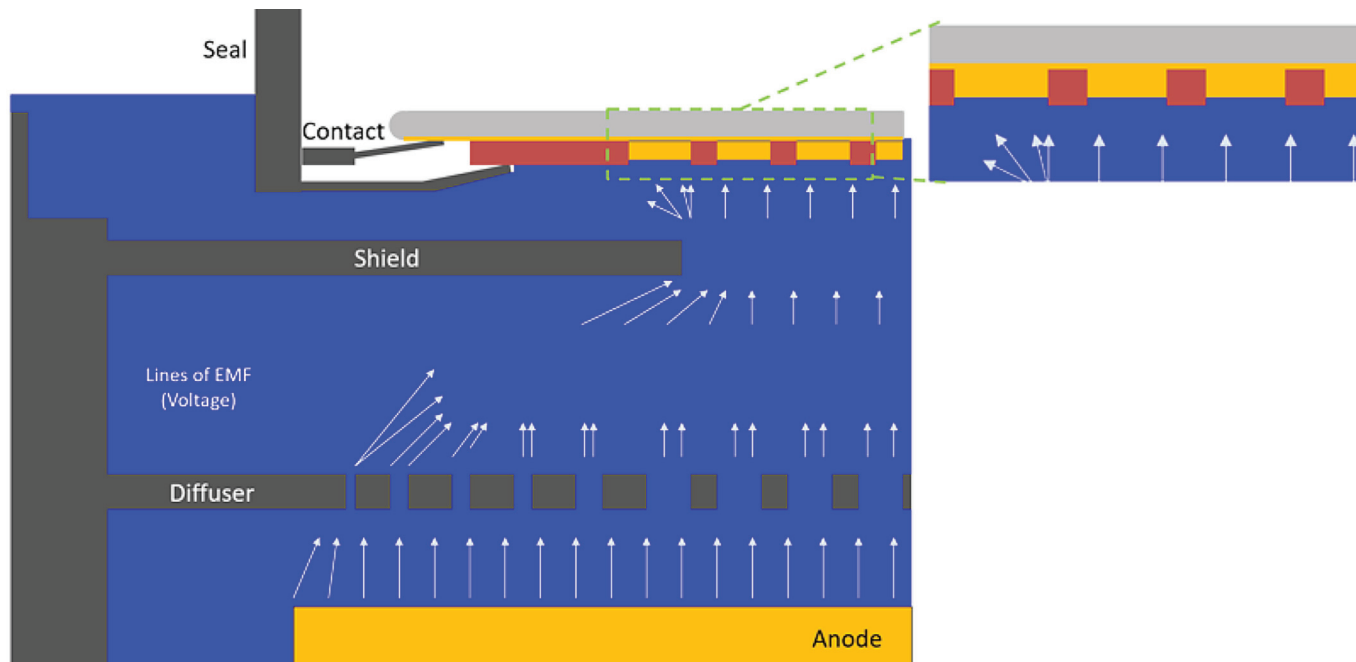


Figure 10. Current crowding at plating seal – with shield

Key Factor: Fluid Flow Profile

The second factor mentioned above, following electric field profile, is the fluid flow profile. In many plating systems, there is only one process adjustment available to control this critical factor and that is flow rate.

Many plating systems used in the industry immerse a wafer vertically into a plating solution and flow the electrolyte past the static wafer. The local fluid vectors of the electrolyte determine the local thickness of the diffusion layer. Faster fluid velocity will thin the diffusion layer and increase plating rate. Slower velocity results in lower plating rates.

Unfortunately for users of such systems, the best uniformity comes when the flow across the wafer is near laminar because the fluid dynamics are more uniform. However, as we discussed earlier, reduced agitation means a lower limiting current density, which means that a low current density must be used, which means a very low plating rate will occur. Speeding up the flow rate results in highly non-uniform fluid flow profile, resulting in increased non-uniformity. In other words, in immersion plating systems, the operator must choose between high plating rates and good uniformity.

The Solstice plating reactor, on the other hand, uses a Rotating Disc Electrode configuration wherein the wafer is immersed face down and spins throughout the plating application. These two design elements result in far superior uniformity of plating due to some key aspects of fluid dynamics.

The behavior of liquid moving across a submerged, rotating disc, is subject to very definite and inherently uniform dynamics. This is because the spinning disc, via centripetal force, drives liquid across its surface from center to edge. This makes complete sense. However, the liquid is incompressible, creating a no-slip condition at the surface. This means that a unit volume of liquid that exits outward from the wafer surface must be instantaneously replaced by an identical volume. This volume cannot come entirely from the wafer surface further in toward the center because that smaller radial area cannot completely replace the departed volume. The departed volume must be replaced in part, and in a very specific quantity, from the bulk fluid. This dynamic sets up a fluid profile in the cell whereby the spinning wafer pumps fluid to its surface forming an incredibly uniform

“plume” (see Fig. 11). The surprising result is that the streamlines which form on the surface of the spinning wafer never change shape no matter the rotational speed of the wafer. Whether 10 rpm or 250 rpm, the streamlines truly retain their exact shape. And herein lie the great benefits of the rotating disc electrode plating system. It is inherently prone to uniform plating.

Now, while the streamlines do not change shape, the velocity of fluid moving along the streamline does change with wafer rotation rate, and thus modifying the rpm does still have an impact on plated film uniformity. However, its impact is a very convenient one because the effects are perfectly radial and subject to the plume from the bulk chemistry which imposes an inherent fluid flow gradient across the wafer surface. In other words, the mode of non-uniformity that is possible in a rotating disc electrode system as regards fluid dynamics is already extremely uniform, and is almost perfectly tunable by modifying wafer rotation rate.

We hope this document has provided you with new or improved knowledge around electrochemical deposition for use in the manufacture of semiconductor devices. If you have questions, please contact us at c1tdc@classone.com.

Figure 11. Naturally uniform motion of fluid across a rotating disk

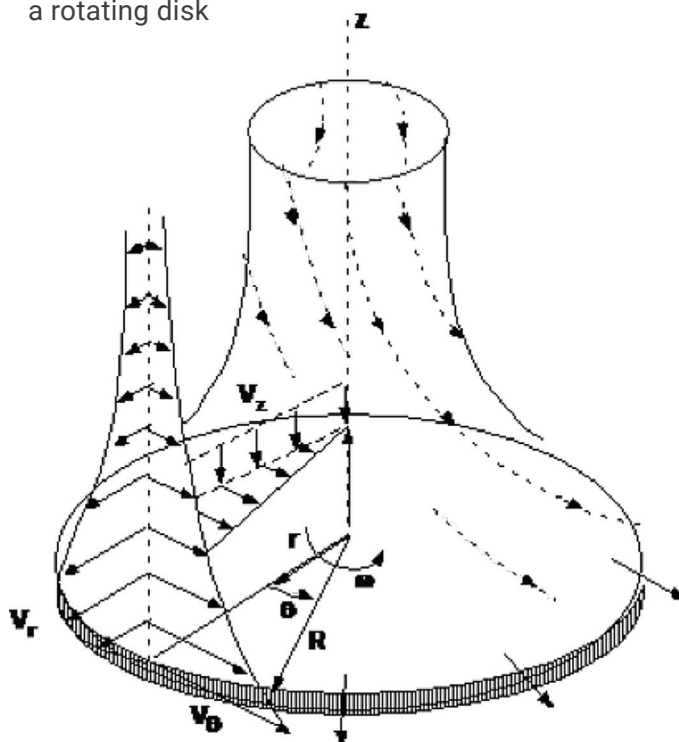


Illustration: Schlichting, Hermann (1960). Boundary Layer Theory. New York: McGraw-Hill.