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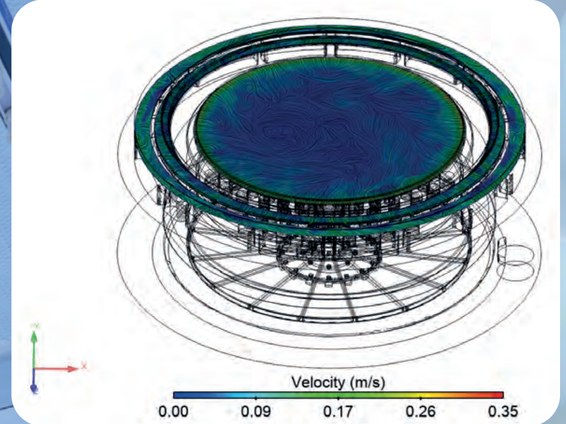

ClassOne simplifies metallization while improving On-Wafer performance

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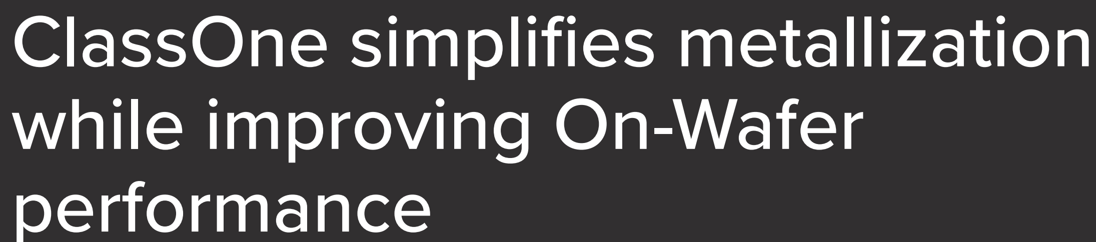


ClassOne simplifies metallization while improving On-Wafer performance

Reducing transistor size to increase performance has driven semiconductor manufacturing since Moore’s Law was first articulated. Only a handful of companies still pursue this; many others look to new device types and architectures that do not depend on shrinking transistors or increasingly complex and expensive equipment. ClassOne Technology is a leader in the anti-complexity revolution that champions high performance and cost-effective throughput.

BY JOHN GHEKIERE, VICE PRESIDENT, PRODUCT AND TECHNOLOGY, AND CODY CARTER, PRODUCT ENGINEER, CLASSONE TECHNOLOGY

THE WITHERING MARCH of relentless device scaling described by Moore’s Law has left a mere handful of device manufacturers in that race, with TSMC clearly in the technology lead. When the cost per transistor inflected to become more expensive with each generation, somewhere between 26 and 22 nm nodes, it drove even many of the larger and more powerful manufacturers to alternate paths of innovation and new means of bringing value; GlobalFoundries pivoted boldly into FD-SOI; STMicroelectronics into SiC. The broad expansion of new device types - in short, the ubiquitous adoption of microelectronic devices into almost every aspect of our daily lives - has brought about the More Than

Moore era, where feature scaling is no longer the sole means of device innovation.

This sea change in device innovations has essentially occurred in the wake of feature scaling, in a space of free-mindedness around device architecture and the applicability of manufacturing steps defined by that ceaseless grind. The industry, in a sense, has been able to take a breath, and we now see clearly, perhaps surprisingly, that the pace of Moore drove into unit processes and capital equipment certain complexities that may add little or no value. Whereas More Moore brought an almost exponential increase in complexity to unit processes, More Than Moore, while retaining expectations around on-wafer performance, has kicked wide the door to reducing complexity.

The shift is not only timely; it is critically necessary in very practical ways. As the global race for semiconductor leadership continues to escalate, thousands of new semiconductor jobs are being opened with thousands more to come. It is an expansion not previously seen and its impact is the rapid dilution of experience in the workforce. Now, the complexities of setting up, operating and optimizing unit process equipment becomes a costly, and for many More Than Moore manufacturers, a debilitating challenge. Device manufacturers need the same performance from their equipment, but they need it to be simpler to use.

The truth of the impacts of Moore on complexity was made clear to me, in a previous role, during a visit to a major advanced memory manufacturer to discuss process equipment technology. I had traveled to share some recent development results, aiming to place equipment within a new R&D location within the fab. The senior technology director was pressing me on a particularly nuanced capability that our competitor had and we did not. Adding the capability meant introducing a complicated mechanical system submerged in a concentrated wet chemistry. From an engineering perspective, such a system was not only expensive, but it introduced a dozen new potential failure modes. I explained to him that we had studied that function and its effects in depth and could find no indication of any kind that it provided any benefit. I asked for clarity of its on-wafer benefit. He said, “John, you don’t understand. If I can measure it, then you must control it.”

It became clear. The pace of Moore means that there is simply not sufficient time to investigate everything to complete understanding. Perception of risk is risk, thus, complexity is driven in, even if, in certain cases, that complexity serves as largely an insurance policy against factors that may or may not be important. Better to have the complexity (and cost) than the question.

The More Than Moore crowd are rising in the wake of Moore, where heightened complexity no longer offers assurances. It offers higher cost and more unwieldy process steps; and if it doesn’t bring measurable benefit, then it simply isn’t needed. The opportunities are fruitful. This article will focus on the simplification of electrochemical deposition (we’ll simply say plating), which when compared to the entirety of semiconductor unit processes, already lies somewhere in the middle in terms of complexity. Plating is also broadly and deeply captured by a great host of patents. As a basic technology, plating is already more than 200 years old; yet, as we will show, even its fundamentals are ripe for innovations that simplify operation while not only maintaining on-wafer performance, but improving it.

Plating remains an enabling, cost effective and highly-flexible option for metallization. The means of producing high quality plating and excellent on-wafer results are well established. The principles behind great performance are no longer the domain of one or two providers.

Uniform deposition by plating requires careful sculpting of two key factors: the electric field profile and the fluid motion profile.

As it turns out, the electric field is actually the easier of the two to perfect. Computational Fluid Dynamic modeling (CFD) provides an exceptionally accurate and predictive model around the electric field and its ultimate effects on on-wafer performance, namely film deposition rate. The need here is to deliver a zero-gradient potential at the wafer surface. The electric field wants to be zero-gradient so this aspect of reactor engineering has a lot to do with developing hardware that “stays out of the way.” In terms of the actual state of reactor hardware in the industry, however, the scaling race resulted in over-engineering of plating chambers for most More Than Moore applications and, arguably, many

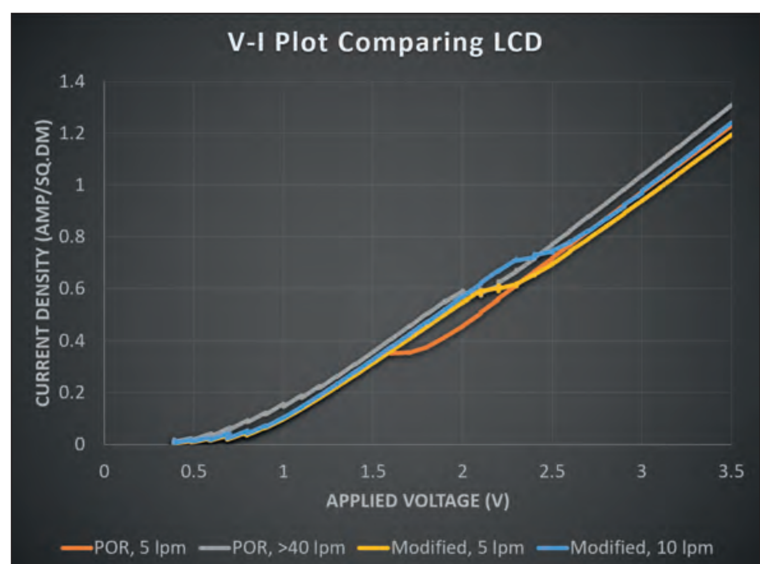
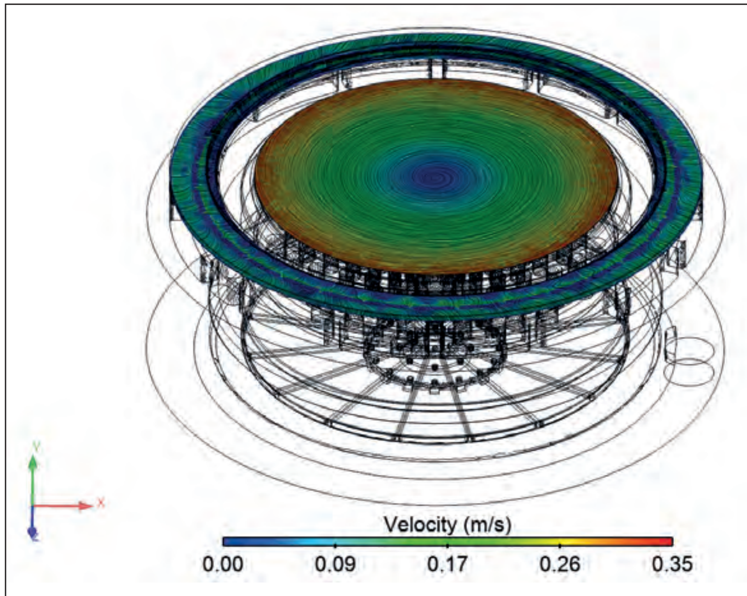


Figure 1: V-I plot comparing LCD of POR condition against modified condition



➤ Figure 2: CFD image of electrolyte at wafer surface

applications at >32nm node.

Anode elevators, mechanically actuated irises and multiple independently controlled anodes provide very clever and interesting control knobs (as an engineer who worked extensively with such systems, I also found them extremely fun to play with). But these features add complexity and hardware costs that provide little to no benefit except in the most extreme use cases. For example, multiple independently controlled anodes do allow for radial tuning of the electric field. But so do physical diffusers made of natural polypropylene. The difference is not in the ability to deposit uniformly - both do. The difference lies in the need (or lack thereof) to adjust dynamically insitu.

Electric field dynamic tuning is very cool. But patently unnecessary for seed thickness above about 100A. A careful reader of this article will note that a uniform potential at the wafer surface does not necessarily mean a uniform current density across that surface. However, looking more closely at the reality of the situation, we find that until scaling drives a sufficiently thin seed material, one that results in a significant potential gradient across the wafer itself, a uniform potential does result in a uniform current density. The multiple independent anodes, as well as mechanically actuated irises, really only find their use in the dynamic condition where a very thin and resistive seed rapidly, typical of the most advanced logic and memory devices, thickens with plating, changing the curve to a flat one. The vast majority of MtM applications, as well as damascene applications at 32nm and above, are applied to wafers with a flat potential profile. It's notable, if you believe the patent landscape, that only one major plating manufacturer engineered multiple anodes into its system, and more notably that the provider with the larger market share was not that one.

So we see that shaping the electric field is readily done and without complexities that bring challenging setup procedures as well as expanding modes of potential failure.

The more challenging factor is the fluid motion profile. The fluid motion profile relates entirely to cation availability. Plating processes result in beautiful, shiny high purity metal films in large part because those processes are run in an "electron-poor" regime. This regime is crippled when the concentration of target cations available at the surface of the wafer is drawn down to become similar to the "concentration" of electrons. In such areas on the wafer where this depletion occurs, the resistance rises, and since the plating system is driving a potential while tuning by an ammeter, the localized current density is lowered and plating slows locally.

The key to ensuring abundant cation supply is to make uniform the time required, at each location, for the target cation to cross the diffusion layer. This can be done by simply slowing the process. But, as a rule, device manufacturers do not like to slow down processes. Again, the inherently risk-averse drive of Moore resulted in a large number of complexities aimed to eliminate questions of cation availability with brute force as opposed to system efficiency.

There is an interesting difference between e-field and fluid motion profile in that the e-field reaches the wafer and "sinks in". The fluid motion profile, by contrast, has to get out of its own way. The fluid that reaches the wafer must turn and go away from the wafer, and it must move past other fluid in order to do so. The challenge here, in terms of supporting the highest possible plating rates, is to sculpt the fluid motion profile in such a way that no bias of motion is produced. A bias in fluid motion vector creates localized and stable differences in diffusion layer thickness, which translate to slightly different times for cations to diffuse. As the current density is increased in order to drive the fastest possible process, so is the consumption of those precious cations.

The limitation is reached wherever that supply becomes sparse and starts to impose higher potential, thus lower current density, thus slower localized plating, and an impact to uniformity. The most prevalent solution to combat this in the industry has been the inclusion of a submerged paddle. While simple in concept, paddles do add to complexity of a chamber. They introduce more moving parts and therefore things that require setup and which have certain modes of failure. They also, obviously, add to the cost of building the reactor, both in terms of materials, machining steps and labor of assembly. In cases where a technician needs to access the interior of the chamber, for whatever reason, there is now the need to get the paddle out of the way of hands and tools. In short, chambers must be disassembled for even relatively

minor maintenance tasks.

Interestingly, as noted earlier in this article, whereas we said that forming the profile of the electric field was easy and amounted to setting it up and then staying out of the way, with paddles, there is something literally placed in its way.

In actuality, the electric field is not manipulated by the motion of the electrolyte. But it is manipulated by the hardware that produces the motion of the electrolyte. Put another way, one can independently model the electric field and the fluid motion profile. And the results of the models accurately predict on-wafer behavior. The two factors really do function independently from one another. This means, in theory, it should be possible to tune them separately. And yet, reactor designs historically bind the two together. After all, the fluid passes through and across the same hardware that the electric field does. The result has been the proliferation of highly complicated reactors driven by the dual constraint of field sculpting and fluid motion formation. Theoretically then, if one can fully segregate optimization of the electric field from optimization of the fluid motion profile, then both can be tuned to best possible state without "getting in the way". And this, it turns out, can be done with a reduction in complexity as opposed to an increase.

The thickness of the diffusion layer cannot be directly measured of course. But a very descriptive proxy is available by use of an V-I graph, which plots voltage as an input and current as the output. Ohm's Law of course states that, for an electrical circuit with a given resistance, current rises linearly with voltage. This is true of electrochemical systems as well, yet with one notable influence. Electrochemical cells involve electrochemical reactions, meaning the electrons are "consumed" in the formation of reaction products, namely deposited metal. When cations begin to become scarce, the resistance of the system begins to rise and the curve starts to flatten out, as shown in Figure 1. This flat region is called the Limiting Current Density (LCD) and it serves as a practical limitation to how fast one can drive a plating system. Approaching this region leads to poor uniformity and ultimately poor deposition.

The LCD of a given system thus serves as a means to compare cation availability between systems. If a modification of a given system results in the LCD being moved to a higher potential, that means the supply of cations has been improved. It further means that the system can be run at a higher current density while still depositing high-quality films.

ClassOne Technology, with MtM manufacturers as its target customer base, has adhered since inception to a design ethic whereby no complexity is added to its Solstice plating system unless actual value is realized. And even having started from this mission of design elegance, continues to uncover new means of advancing on-wafer results while maintaining or even reducing complexity.
In revisiting the principles summarized above, we understood that our paddle-free GoldPro reactor, which already competes with all major plating systems globally for on-wafer performance and feature uniformity, could be improved further in terms of the simplicity in delivering perfectly uniform features across the entire wafer.

Typical adjustments that raise LCD include increasing agitation or increasing temperature. Typically, increasing electrolyte temperature causes certain undesirable side effects and is not a practical option. This leaves agitation and also explains the reason that paddles have been so prevalent in reactor design. Other means of enhancing agitation involve higher wafer rotation rates and higher fluid flow rates. Wafer rotation rate is constrained by two factors: one, it produces radial effects in terms of localized variations in cation availability, thus there is going to be an optimal rotational speed above which uniformity becomes worse again. Secondly, a too-high wafer rotation can establish stable and directional fluid motion, i.e. bias, that results in localized non-uniform plating and lopsided features. Thus wafer rotation rate is not really a viable process knob for substantially increased plating rates.

Sheer fluid flow rate is viable as a process parameter though it bears practical limitations related to pump size as well as fluid evacuation (remember, the fluid has to get out of its own way). If the aim is simplification, which it is, then inclusion of a paddle is not taking things the preferred direction. All of this apparently leaving few options for raising LCD and making room for higher plating rates. ClassOne, through a focused effort aided by CFD modeling, investigated certain passive means of fluid manipulation within its reactor, aimed at producing ample fluid motion in a non-directional

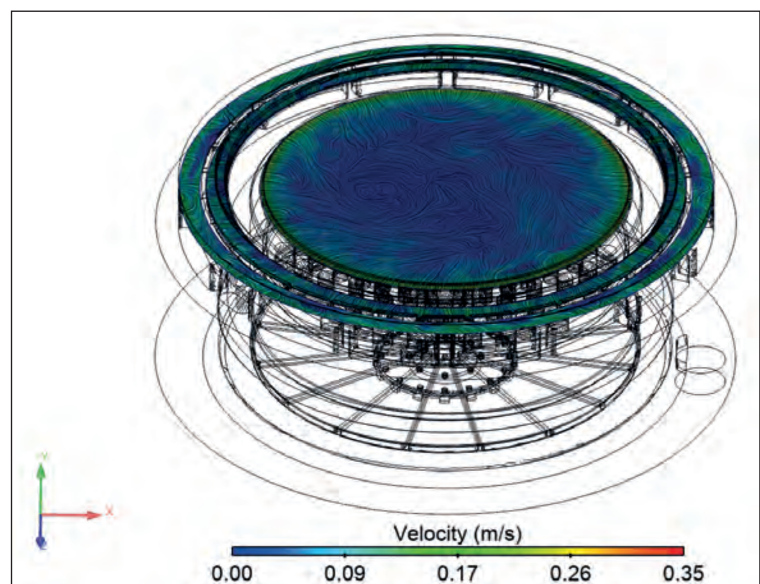


Figure 3: CFD image of electrolyte <1mm from wafer surface showing randomized motion

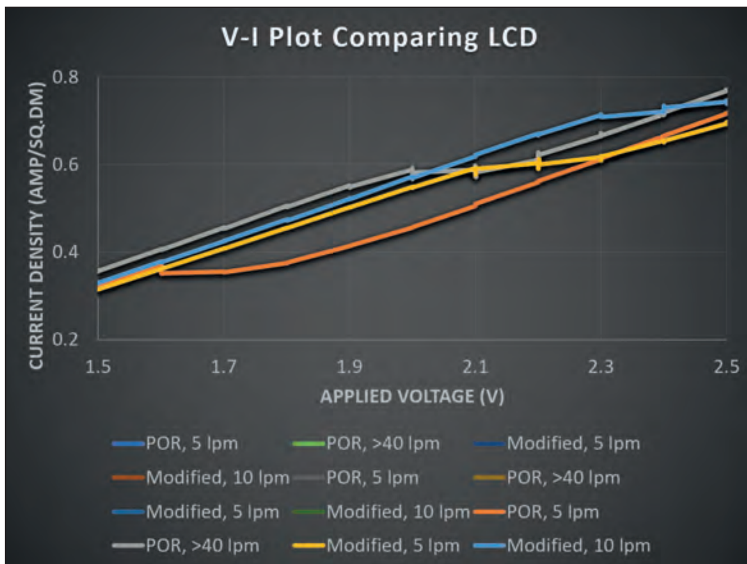


Figure 4: V-I plot zoomed in to highlight increase in LCD using modified condition

manner. Considered more closely, our aim was to transform the observed motion of fluid from the circular motion of liquid attached to the spinning wafer to a random pattern, and to do so as close to the wafer as possible. CFD modeling of various reactor concepts directed the design team to a specific concept that manipulates fluid motion in a passive way (i.e. no paddles or moving parts).

As the model shows, the electrolyte at the wafer surface (d=0) is clearly attached and moving rotationally with the wafer. Yet at a distance much less than a millimeter, the fluid motion is already largely random, leaving no effective bias. (See Fig 2 and 3) Further, the concept increases cation availability, as evidenced by a significant shift upward of the LCD. The LCD is found by initiating a plating sequence in voltage control mode and then periodically raising the voltage setting while recording the current that results.

Using this method, the LCD was found for POR condition which uses a flow rate of >40 lpm. Combined with a specific wafer rotation rate, this POR produces cross-wafer uniformity in gold of <2.5% 3-sigma and a feature uniformity of <1% (max-min / max+min). We then used the same method to find LCD at lower flow rates, including as low as 5 lpm through the system. The lower flow rate on the standard system produces a very low LCD, so low as to be debilitating. In short, this is a process of very low productivity.

Next, by implementing some targeted changes to fluid motion through the reactor, still employing a passive system, we determined that the LCD at 5 lpm flow rate, could be raised again to the level of LCD for the POR at >40 lpm. The conclusion is that, with the targeted modifications to the reactor, we are able to maintain very high cation availability at the wafer surface while decreasing the flow rate by more than 87%! This opens the process window significantly without high flow rates. As a last confirmation of the new approach, we then increased flow to 10 lpm (still a quite low flow rate) and we see that the LCD is actually improved to a value higher than the original POR. (See Figure 4) The conclusion is that greater performance is achieved using a simpler process.

The specifics of this design, while they cannot be disclosed in this publication, also ensure that the manipulation of the fluid motion profile does not interfere at all with the formation and shaping of the electric field. The chamber stays out of its own way. Taking altogether, we confirmed that exceptionally high cation availability is possible at significantly low flow rate using a passive means of fluid motion control, i.e. no paddle or other submerged moving parts. Further, we demonstrated we were able to achieve this profile without interference to the electric field distribution.

The work shows that there is ample room, particularly among More Than Moore device manufacturers, to not only maintain competitive on-wafer performance, but to improve on it, while simultaneously eliminating complexities in the process system. This results in lower costs on equipment, lower costs on maintenance, and a far simpler system to operate at a time when the industry is experiencing rapid dilution of experienced workforce.

And this is just the beginning.

For additional information, please visit: https://classone.com/reactor-and-platform-innovations-advancing-our-plating-technology/#GoldPro

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