Process Application Note
PAN101

Electroplating Fundamentals: Optimizing Cross-wafer Uniformity

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Introduction

ClassOne has developed this Advanced Semiconductor Plating series to provide theory and practice guidance for today's electroplating engineers and operators to help them optimize their processes.

This series is arranged in four parts:

Part 1: Key Fundamentals and How to Dial In Target Plated Thickness
Part 2: Factors Affecting Localized Plating Rates and How to Optimize Cross-wafer Uniformity
Part 3: Wafer and Feature Effects and How to Optimize Feature Uniformity
Part 4: System Level Factors and How to Establish Repeatable Plating Performance

Part 1 of this series provided the basic fundamentals for establishing target plating thickness. This second part focuses on the uniformity of plating within a wafer and the physical principles that apply.

Electroplating Uniformity Basics

Fundamentally, the uniform deposition of metal within and across a semiconductor wafer is influenced by two primary factors:

- The definition and control of the electric field profile
- The establishment and maintenance of cation availability.

Because of these factors, different electroplating systems can differ significantly in their on-wafer performance. The architecture of a specific plating system can fundamentally enhance – or limit – its achievable performance.

One example of limitation is the simple wet bench, which plates to a static wafer. Its architecture limits its uniformity to no better than approximately 10% uniformity within-wafer.[1]

Some of today's more advanced electroplating systems, however, are specifically designed to enhance on-wafer performance. And this can enable them to more readily produce class-leading levels of uniformity.

That being said, this series aims to be explanatory, informative, and helpful to a broad range of industry technicians and professionals, regardless of the specific brand or type of plating equipment they are using. The primary purpose of these papers is to present the fundamental concepts and principles that are the basis for superior electroplating performance.

[1] There are a number of common ways to calculate within-wafer uniformity. The 10% value stated here is generally applicable to uniformity calculated as 3-sigma mean/standard deviation or a range/2*mean.

Electric Field Profile

Parallelism and Radial Symmetry

The application of a potential to the reactor system produces an electric field. This field propels cations, the metal ions that react to form plated metal, toward the negatively-charged wafer; and likewise, it draws electrons toward the positively-charged anode. The magnitude of the force an ion experiences correlates directly with its proximity to the electrode and the current applied to the electrode. As positive ions (+) are produced at the anode (+), they are repelled from the anode and drawn toward the wafer (-).

This proximal reality between anode and cathode/wafer is critical in the architecture of plating systems. A static wafer that is not perfectly parallel to its anode will experience an inherent linear non-uniformity due to mechanical proximity. This error can only be corrected by tighter mechanical design.

Whereas a static wafer system would exaggerate such an imperfection, a rotating disc system would serve to commit such inequity to radial symmetry. In other words, such imperfection of parallelism would be completely subjugated to a radial consideration. This is simple geometry, and, with a spinning wafer, simple to overcome.

Thus, parallelism between the wafer and anode matters universally, since a percent of difference in this distance from one side to the other would result in a similar percent of difference in the magnitude of the field and thus, a different plating rate for a given radius.

However, by using a spinning cathode/wafer, that difference in plating rate becomes perfectly, geometrically radial. This is critically important.

And, because all of the commensurate knobs of a rotating-disc system, such as Solstice, are inherently radial, the corrections align perfectly to the imperfection. This means that, mathematically, because all the imperfections regarding uniformity are radial, then, since all the correction factors are radial, there is inherent alignment, mathematically, between error and correction. So, hardware perfection is not a fundamental requirement for process perfection if the system is equipped to spin the wafer. In a spinning-wafer system, imperfections in current density may be corrected by recipe and do not depend on the extremely precise machining of plastic parts.

Current Density Distribution Across the Wafer

The wafer, having a negative charge, draws cations toward it, as shown in Figure 1. For a finite cathode, the electric field extends perpendicularly to the wafer surface at the center, gradually changing in angle toward the edge of the wafer. As the electric field is a cumulative effect of the entirety of the charged surface, the field is also, in actuality, strongest toward the center of the wafer. With no consideration given to mass transfer, fluid dynamics, reactor shape, or plating terminus, plating will be fastest at the center and decrease toward the edge of the wafer. Such is the fundamental behavior of the electric field independent of other considerations. As we will see, there are many additional considerations.

As established earlier, current density drives the rate of deposition. Thus, the first consideration in producing a uniformly plated film across an entire wafer is to ensure uniform distribution of the electric field within the reactor.

Figure 1. Electric Field of a Semiconductor Wafer

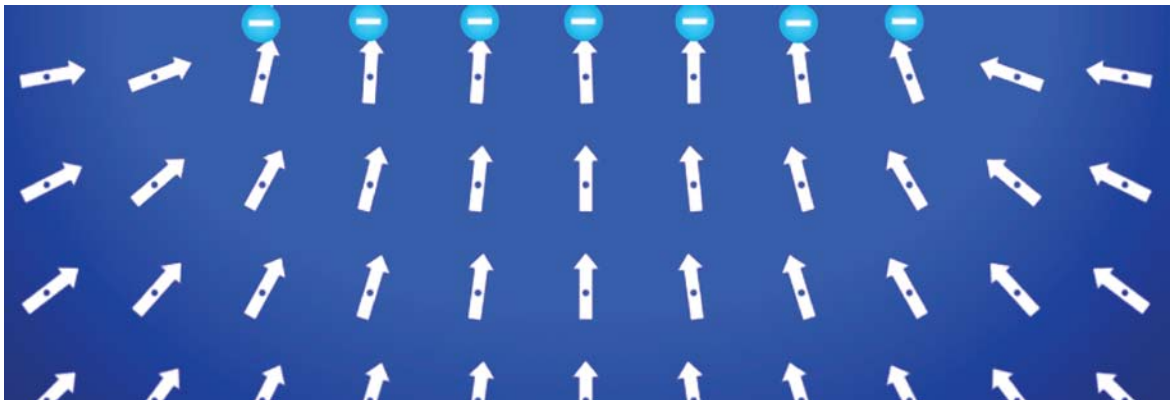


Figure 2 shows a portion of a wafer submerged into a plating electrolyte in preparation for plating on it. The full electrochemical cell is depicted including the contact points where the cell electrically connects to the seed layer of the wafer. The seed layer is necessary to carry electric current to all areas of the wafer. In the image, the wafer is depicted in three meaningful regions: the wafer edge (where the cell makes electrical contact between the power supply and the wafer), the mid-radius, and the center of the wafer.

As discussed in the first paper of this series, Ohm's Law applies to electrochemical cells. Accordingly, the current density incurred at each point on the wafer, which must be the same as each other to achieve uniform plating, is dependent on the voltage and resistance particular to each location. As the image shows, the edge of the wafer is much closer to the electrical contacts than the mid-radius and much closer than the center. Therefore, the edge of the wafer will experience a resistance through the seed that is lower than the resistance at mid-radius, which is lower than the radius at wafer center. This is because the current will need to pass through the seed across a distance moving from edge to center.

In application, however, we find the actual difference in resistance is very low and, in fact, negligible because the typical seed layer is sufficiently thick that its sheet resistance is well within the "bulk sheet resistance" regime. So, to produce an electric field profile conducive to uniform current density across the wafer, it is necessary to produce the same voltage at all points across the wafer. In other words, the field profile produced by the reactor should have a uniform potential across the entire diameter of the reactor.

It is noted that for very thin seed layers, or seed layers composed of highly resistive materials, the wafer will impose a potential gradient across the incoming wafer, which diminishes as the thickness of plated metal increases and sheet resistance falls. This dynamic shift in potential gradient across such wafers can be an important consideration for certain advanced feature plating applications, but this will not be covered within the scope of this work.

The cumulative effect of electric fields means that simple empirical design work can lead to a nominally uniform electric field. An advanced plating reactor such as the Gen4 from ClassOne can be designed to provide state-of-the-art uniformity for multiple applications. For this reason, the Gen4 reactor was designed using computational fluid dynamic (CFD) modeling to ensure highly uniform distribution of the field at the location of the wafer within the reactor (Figure 3).

The uniform distribution of the electric field across the wafer produces uniform potential across the wafer and in the case of a closed circuit, uniformly distributed current across the wafer. This defines a uniform plated layer across a wafer.

The description of the electric field to this point has been intentionally general and has taken no account of the very important manipulations, inherent and intentional, that contribute directly to uniformity in actual plating steps. These critical details will be covered in later sections of the paper.

Figure 2. Current Distribution Through a Wafer

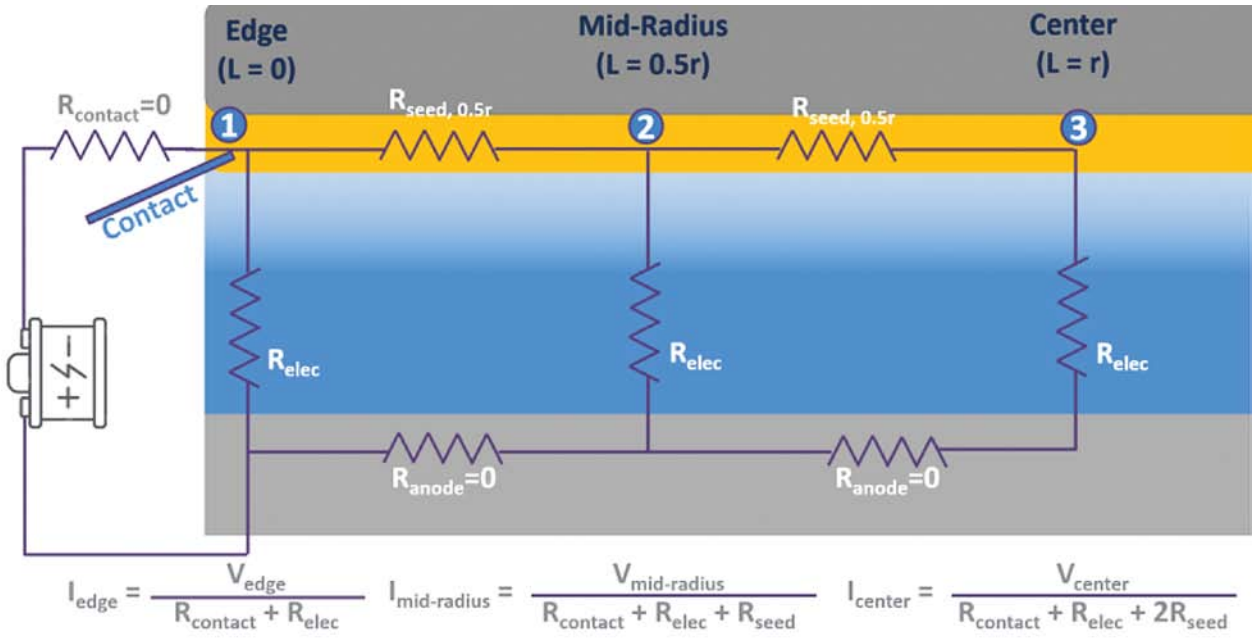
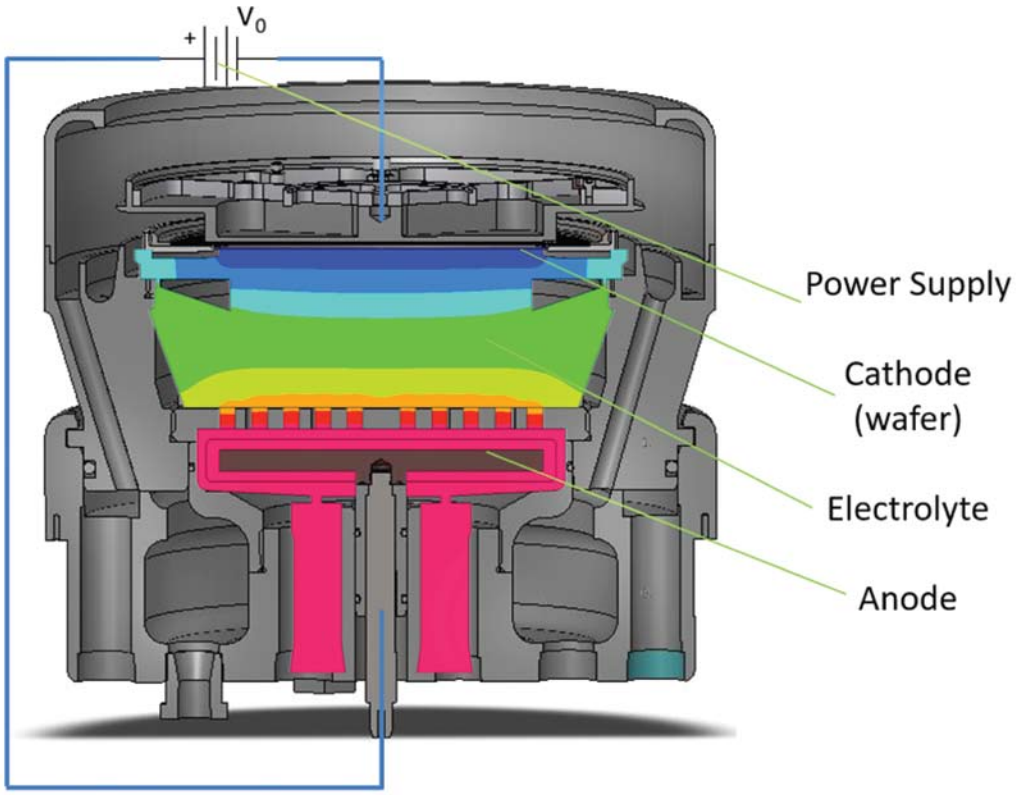


Figure 3. Electric Field Profile in Solstice Reactor (CFD Model



Cation Availability

Cation availability is the second factor that must be engineered properly to ensure uniform metal deposition. The two most important considerations are: cation concentration in the bulk and cation availability at the diffusion layer. The first, which is in the domain of bath formulation and maintenance, will be treated in brief. The second, which is more directly involved in uniform deposition, will receive expanded study here.

Cation Concentration in the Bulk

Semiconductor plating has brought about the development of many specialized and highly reliable plating chemistries. A fundamental requirement of each is that the chemistry mixture be developed around efficient cation concentrations with additives that ensure stability over a practical consumption rate and bath life. Such quality can be expected from the primary vendors of state-of-the-art semiconductor plating baths and this paper will not discuss in detail the vast knowledge base around plating chemistry design. However, as more and more device types are migrated to the manufacturing approach of the semiconductor industry, plating electrolytes developed around industrial uses are frequently being tried in the semiconductor sector. Proper reactor design provides the flexibility to produce semiconductor-grade results from industry-grade plating chemistries.
Having begun from a known good concentration of cations that supports efficient plating of quality metal films, the next consideration is the maintenance of that bulk concentration within a reliable window. This topic will be covered in detail in the section on wafer-to-wafer plating uniformity in Part 4 of this series. Suffice, for now, to say that cation bulk concentration must be maintained.

Cation Availability at the Diffusion Layer

As previously stated, quality electroplating of metals requires that the system operate in an electron-poor condition, such that the reaction rate is limited by, and thus defined by, the rate of the flux of electrons, i.e., by the current. Again, in this line of thinking, electrons serve as the limiting reagent in the reactions involved in deposition.

Given this practical view of the electron supply, it is then understood that cations serve as an excess reagent for the same set of reactions. However, given the possibility of variation in conditions across a wafer, this case cannot be assumed at all locations. Indeed, a supply of cations within the specified concentration of a given plating bath, as covered in the preceding section, is not sufficient to ensure an ample supply of cations at all times, at the wafer surface, across the entire wafer, and within a specific feature.

The reason such assumptions cannot be made is mass transfer, which refers simply to the motion of a given material from one place to another. In the present consideration, mass transfer will be regarded strictly as the motion of aqueous metal cations to a given point of reduction at the surface of a wafer, since this consideration is fundamental to plating rate and thus, to uniformity. As this section will show, several factors influence mass transfer rates throughout the system.

At the simplest level, good mixing in the electrolyte bulk is essential for a number of reasons, not the least of which is to maintain homogeneity of the electrolyte. For this reason, most semiconductor reactors provide for active agitation of the electrolyte with a focus toward turbulent flow at the wafer surface. Most typically, the electrolyte is recirculated through the reactor from a reservoir so that the small percentage of electrolyte depleted within the reactor by deposition is replenished from an abundant supply held to target concentration. As mentioned, the maintenance of the bath will be covered in Part 4 of this work.

Good mixing, while necessary to maintain a homogenous bulk solution at target concentration, nevertheless is not sufficient to accurately control cation availability at the actual surface of the wafer because of the possibility of diffusion differences across the wafer.

The Diffusion Layer

As a viscous fluid moves across a surface at some velocity, it produces a motion profile whereby the velocity decreases asymptotically from the induced velocity of the bulk to a velocity of zero against the actual surface. The layer of fluid that is slowed by this effect is called the boundary layer.

The thickness of the boundary layer (the distance across which the velocity is slowed by interaction with the surface) depends on, among other factors, the velocity of the fluid and its turbulence. A higher velocity and more laminar flow produce a thinner boundary layer. While laminar flow contributes to a thinner boundary layer, it becomes turbulent the longer it flows against the surface and if it encounters any irregularities on the surface, irregularities such as photoresist pattern. Turbulent flow, while producing a thicker boundary layer, is less susceptible to eddies created by features on the surface.

For the purpose of efficient plating, it is desirable to have as thin a boundary layer as possible to supply the bulk concentration of cations as near to the wafer surface as possible. However, the physics dictate that ultimately there will exist an essentially stagnant layer of some thickness through which the cations must pass by sheer diffusion, which is much slower than convection and mixing. In electrochemistry, the defining term for this layer is the Nernst diffusion layer, which is the "region in the vicinity of an electrode where the concentrations (of ions) are different from their value in the bulk solution."[2]

Cations must cross from the region of homogenous bulk concentration, through the stagnant diffusion layer, to the surface of the actual wafer to participate in cathodic reactions there. This motion is called diffusion, and the time required for cations to traverse the diffusion layer is significant for the sake of uniform deposition. For the purposes of this paper and its focus on practical knowledge in electrochemical deposition on semiconductor wafers, it is sufficient to consider the 'velocity' of a given cation across the diffusion layer to be constant within a controlled plating process. In other words, a cation of specific makeup travels across the diffusion layer at a set speed determined by its specific diffusion coefficient. More simply, the total time required for a given cation to traverse the diffusion layer depends directly on the thickness of the diffusion layer.

Because the thickness of the diffusion layer is practically bounded on the low end (i.e., it cannot be less than zero),

[2] IUPAC. Compendium of Chemical Terminology, 2nd ed. (the "Gold Book"). Compiled by A. D. McNaught and A. Wilkinson. Blackwell Scientific Publications, Oxford (1997). Online version (2019-) created by S. J. Chalk. ISBN 0-9678550-9-8. https://doi.org/10.1351/goldbook.

its thickness will asymptotically approach some minimum value. One can see, then, that providing a uniform and thin boundary layer contributes to cations traversing the diffusion layer in the same amount of time at all locations, thus maintaining the same deposition rate at all locations, and thus plating uniformly at all locations. Considering that the velocity of diffusion is constant, if the diffusion layer is not of uniform thickness at all locations, the time required to reach the wafer surface will be longer where the diffusion layer is thicker and shorter where it is thinner. Thus, a non-uniform fluid velocity profile across a wafer surface will result in a non-uniform diffusion rate and thus, a non-uniform plated layer.

It follows that a semiconductor plating reactor in pursuit of uniform deposition should provide a uniform fluid motion profile across the wafer. The description here is of fluid motion relative to the wafer surface; therefore, two considerations are evident:

- The motion of the fluid as caused by the fluid delivery system
- The motion of the wafer with respect to the fluid in the reactor

As mentioned previously, it is typical of a semiconductor plating reactor that chemistry be recirculated through the chamber. Now, too, we must recognize the critically important issue of wafer motion, which has profound impact on plated film uniformity. And it bears noting that certain plating system designs make no provision for this key factor!

Electrolyte Motion and Flow

The velocity of electrolyte relative to the wafer surface must be sufficiently high to produce a diffusion layer thin enough that the time it takes for cations to diffuse to the surface is not so long that it constrains the reactions of deposition. Otherwise, cations risk becoming the limiting reagent in some areas around the wafer.

For some applications, where the mobility of the cation is very high, producing a diffusion layer that is “thin enough” can be achieved simply by applying a high velocity of chemistry across the wafer surface. State-of-the-art copper semiconductor electrolytes are a good example of this. The cupric ion diffuses relatively quickly across the diffusion layer, as opposed to the gold complex ion, which diffuses very slowly.

This is a critical consideration in equipment selection since it is a fundamental aspect of the system architecture. Consider vertical rack plating equipment for relatively simple copper plating applications where uniformity has a very practical lower limit of around 10%. This limitation is fundamental because stationary wafer systems force a tradeoff between plating rate and uniformity. By flowing high velocity through the system, turbulent flow interactions are generated at the wafer. The typical configuration of such systems is that chemistry is delivered from the bottom of the chamber, translates vertically across the wafer surface, and cascades out at the top of the chamber. The result is that the flow profile changes from the point of delivery to the other end of the wafer. (This discussion currently ignores the effects of features, which will be covered in Part 3 of this series.)

Good mixing is achieved, and the diffusion layer is thinned, but turbulent flow is inherently non-uniform, which will cause the diffusion layer to be of different thickness across the wafer. The turbulent flow will produce high plating rates since the nominal thickness of the diffusion layer will be low; however, the deposition will not be uniform. Thus, high plating rate is achieved but at the cost of poor uniformity. Slowing the flow will produce a more uniform relative fluid velocity, but it will result in a thicker diffusion layer. This yields a relatively uniform deposition but puts limits on the plating rate.

Alternatively, a static wafer can be oriented horizontally, such that the plating side of the wafer is facing downward, into the flow of electrolyte. In this orientation, the nominal vector of the electrolyte encounters the wafer perpendicularly. This helps to undo some of the limitations of the bottom-to-top flow path of static vertical plating cells, but it still does not mitigate the shortcomings of the diffusion layer thickness being driven strictly by the flow profile generated by the chamber design. Such a chamber would likely require very complicated design to improve the flow profile, and would necessitate extreme precision in the dimensional elements of the assembly. Yet, the tradeoff of high flow vs. uniform relative fluid velocity would still remain. Even putting great expense into design and manufacture, optimum uniformity would still not be achieved.

Wafer Motion

However, it is possible to take advantage of physics and conform the electrolyte flow profile perfectly to the shape of a wafer – to produce a perfectly radial flow profile without extreme design and manufacturing costs for the reactor. This can be achieved by spinning the wafer.

Spinning the wafer takes advantage of the complex physics of a submerged rotating disc. The depths of this area of study are considerable and form the basis for much of electrochemical analytical science. For the present work, we will focus on the practical implications that apply to uniform film deposition.

For the moment, the electrolyte flow induced by recirculation through the chamber will be ignored. For the purpose of isolating the benefits of a rotating disc as regards uniformity, we will assume the flow of electrolyte delivered to the wafer to be zero or negligible. For reasons already discussed and others to come in this work, a stagnant or nearly stagnant flow rate is, of course, not recommended.

Behaving as a rotating electrode, a spinning wafer acts as an effective, if inefficient, pump. This becomes easy to understand in light of the above discussion of boundary layer and diffusion layer, coupled with the fact that liquids are incompressible. The spinning wafer surface, because it is submerged, is completely covered in liquid. Figure 4 depicts a CFD model showing liquid fraction of 1.0 at the wafer surface, meaning that liquid is fully attached to the wafer surface at all locations.

This means that any displacement of electrolyte from any unit area of the wafer must be instantaneously replaced in its exact volume by more electrolyte. This is known as the no-slip condition. Since the wafer is spinning, viscous forces will cause liquid to move radially outward across the wafer surface until it reaches the edge, where it will exit from the wafer surface. Of course, this description is only briefly covering a great deal of deep science; however, for our purposes, it is sufficient to highlight the fact that in spinning a submerged wafer, fluid motion across the surface, driven by centripetal force, causes displacement of the surface liquid.

Regarding the geometry of a spinning wafer, one can imagine a specific width area around the edge of the wafer that is exiting the edge of the wafer. That width cannot be fully replaced upon its exit by the same unit of width ring adjacent inward of itself. The area of the adjacent ring is smaller. But the no-slip condition ensures that volume is instantaneously replaced; thus, the additional fluid volume is made up from the bulk fluid. Extrapolating this inward, from edge to center, it can be seen why the effect is amplified as fluid moves across the entire wafer.

Figure 4. Cross-section of Gen4 Plating Reactor, CFD Model, Showing Liquid Fraction (proprietary elements obscured)

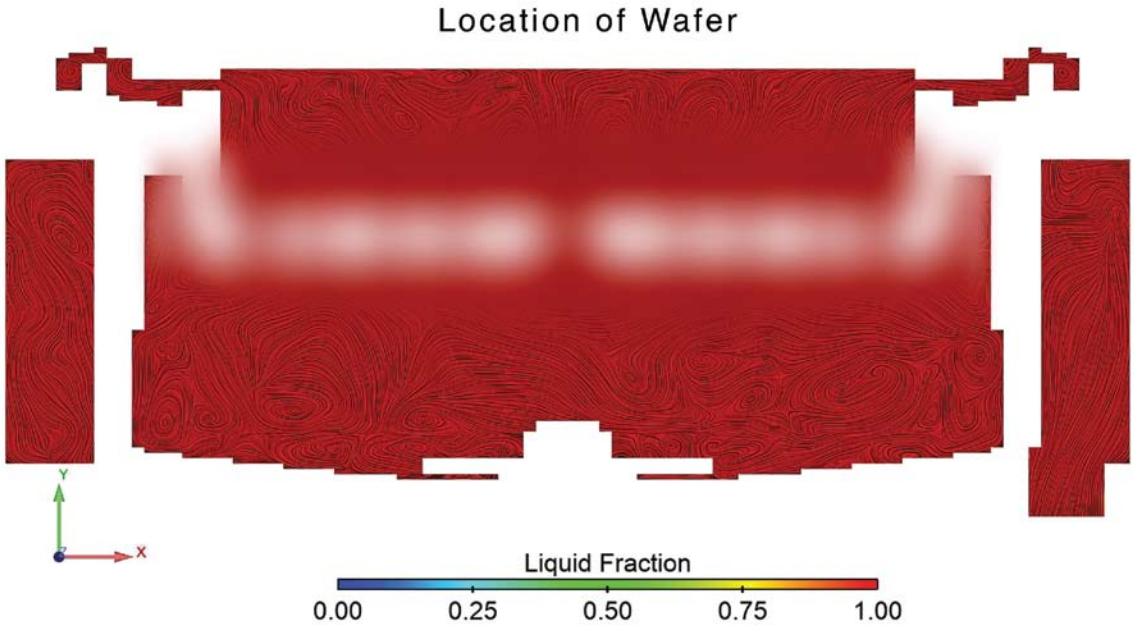
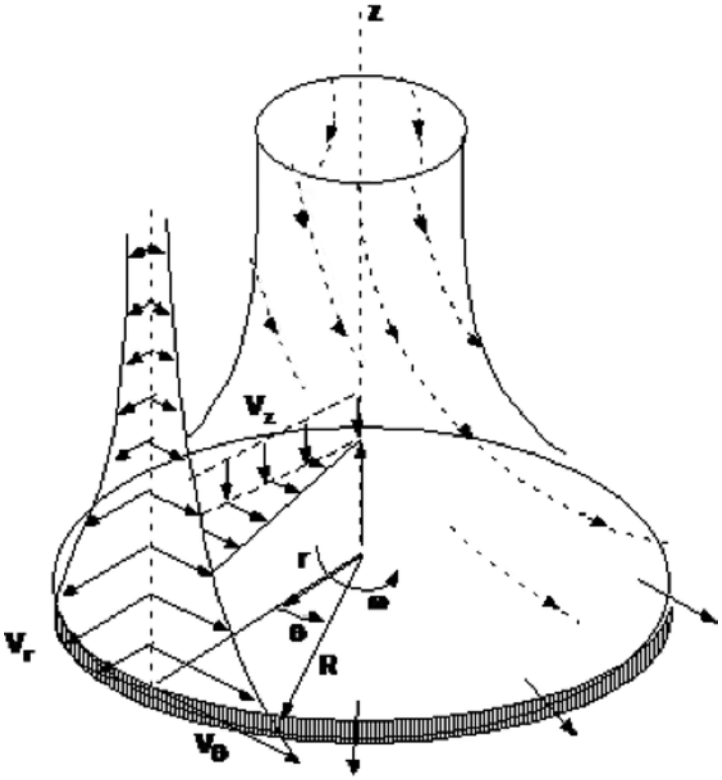


Figure 5, from the seminal text, *Boundary-Layer Theory* by Dr. Hermann Schlichting, illustrates the fluid dynamics. A plume of electrolyte motion is formed within the bulk. One can see that the plume, when generated in a nominally symmetric, cylindrical chamber cavity, will develop a profile that is perfectly radial, perfectly centered to the axis of rotation. In other words, the wafer's motion defines a flow profile that is inherently tuned to uniform distribution across the wafer surface. The task of the hardware is simply to have radial symmetry that does not interfere with what physics will otherwise accomplish with perfection. ClassOne's Gen4 electroplating reactor takes advantage of the effects described.

Figure 5. Fluid Dynamics, from *Boundary-Layer Theory* by Dr. Hermann Schlichting



Electrolyte Motion and Flow:

From the above discussion, we see that wafer motion is extremely important in determining the effects of relative fluid motion on plated film uniformity. This is not to suggest that fluid motion through the plating system is not important. However, spinning the wafer reduces the criticality of the system's flow profile.

In a static wafer system, many factors will be unavailable for tuning due to the system's architecture. The hardware that determines the flow profile will either have no adjustability or very limited adjustability. Therefore, the only effective tunable parameter is total flow rate. For a static wafer system, the flow rate would need to be optimized empirically to strike a balance between uniformity and plating rate, and the system would be sensitive to changes in actual electrolyte flow rate.

However, in a system equipped to spin the wafer, the scenario for flow of the electrolyte through the reactor is fundamentally different. In such systems, the impact of the fluid flow rate is secondary to wafer motion and much less sensitive as a controlling factor. Note that for a high-quality spinning-wafer plating system, the flow rate delivered to the system can be reliably provided from equipment documentation and should require no adjustment or fine-tuning at all.

In the case of ClassOne's Solstice system, for example, the user can expect to receive published Process of Record documents that specify a standard electrolyte flow rate for a given application. This number can simply be entered into the tool software without empirical validation. ClassOne will also provide a firm rpm setpoint, since the effects of the setting are both precise and repeatable from system to system, given that any minor change in overall flow profile will be overcome by the physics of the rotating disc.

Limiting Current Density

As previously discussed, an electrolytic cell, comprising a circuit, is subject to Ohm's Law (V = IR), which would normally identify a linear relationship between the current and the voltage for a given, constant resistance. However, the electrolytic cell adds a complexity that modifies this otherwise linear relationship. That complexity is unintended electrochemical reaction.

As current density is increased, the consumption rate of cations increases. At some point, the availability of cations at the surface becomes insufficient, since the rate of consumption of cations (i.e., plating) approaches the rate of replenishment of cations. The system begins to shift away from its proper electron-poor condition, and if cations are not abundantly available, electrons will begin to interact in other ways, initiating side reactions that result in poor-quality deposits.

As shown in Figure 6, this condition causes the linear relationship of V:I to draw flat. This point, known as the Limiting Current Density, or LCD, is characterized by a constant current density despite an increasing voltage. Returning to Ohm's Law, it is then understood that the resistance of the system is now increasing.

The point at which LCD is reached is dependent on several factors, and it may be possible to maneuver LCD to a higher or lower current density by adjusting various parameters. As shown in Figure 8, increasing electrolyte temperature and/or agitation of the fluid at the wafer surface can increase the current density at which LCD is reached. Temperature increases the kinetics of the plating reaction(s). Agitation thins the diffusion layer, thereby increasing the effective replenishment rate of cations at the diffusion layer. Likewise, increasing the concentration of cations in the bulk solution can increase availability of cations at the diffusion layer. In all cases, the adjustments maneuver the process back to an electron-poor condition, moving the cell back into charge control region.

Figure 6. Voltage-Current Density Relationship

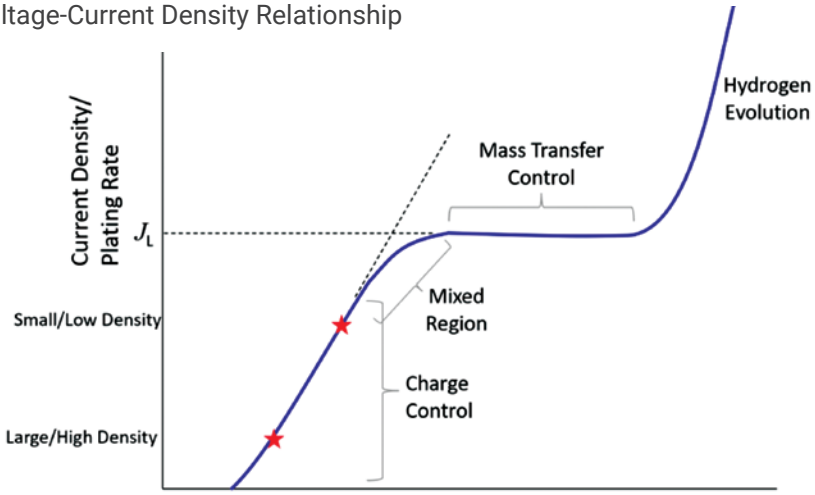
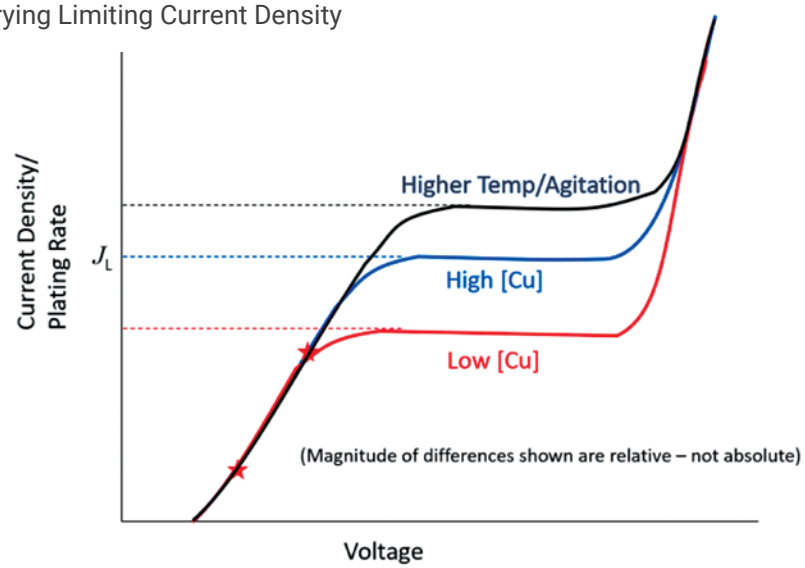


Figure 7. Varying Limiting Current Density



Dialing In Cross-wafer Uniformity

This section gives recommended guidance for dialing in cross-wafer (or within-wafer) uniformity. Note that the following information covers uniform plating *on blanket seed wafers*. Part 3 of this series covers specifics for common *feature* types.

We begin with specific guidance for ClassOne's Solstice plating reactors. Following that is more general guidance for other single-wafer, horizontally-oriented plating systems. It is best if the reader can begin with a known functional starting sequence. If the system in use is new or the user is new to it, then some time should first be spent in establishing a functional starting point, whereby the system is being operated as designed.

The best thickness measurement pattern for optimizing cross-wafer uniformity is generally the diameter scan (Figure 8), which is simply a line of measurements starting on one side of the wafer and running across to the other, often with a higher density toward the wafer edge where more variation is possible. If using a 4-point probe for thickness measurement, please note that measurements from such systems can be inaccurate within 2mm of the edge of the measured film.

Figure 8. Example of a wafer diameter scan

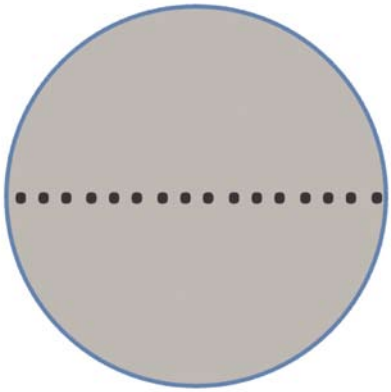
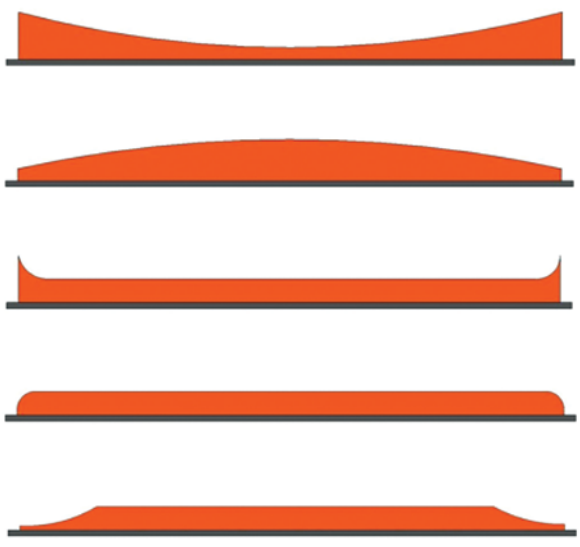


Figure 9 illustrates typical wafer diameter scan profiles and provides guidance on correcting the problems that may be indicated.

Figure 9. Typical diameter scan profiles and associated causes



- Problem: RPM too high
- Solution: Decrease RPM

- Problem: RPM too low
- Solution: Increase RPM

- Problem: Shielding insufficient
- Solution: Decrease Working Distance

- Problem: Shielding excessive
- Solution: Increase Working Distance

- Problem: Bubble trapped on entry
- Solution: Reteach Entry

Dialing In Cross-wafer Uniformity on a ClassOne Solstice Plating System

1. A Process of Record (POR) document, available from ClassOne, will provide a clear definition for a starting point. Or contact the ClassOne Applications Group at c1tdc@classone.com to request the POR document.

2. Refer to the first paper in this Plating Fundamentals series (available at classone.com/tech-papers/) for assistance in establishing the proper settings and recipe to achieve target plated thickness. The key factors for establishing cross-wafer uniformity are: electric field profile and fluid flow profile. Both are readily optimized through intuitive settings.

3. The series of adjustments on a ClassOne reactor are straightforward:

■ **Recipe**
Ensure accurate entry of your ClassOne recipe from your POR document. Contact ClassOne if you need an updated copy, or if you have a legacy recipe to update.

■ **Diffuser**
Set diffuser according to electrolyte. This information is available from your ClassOne POR or by contacting ClassOne. If desired, finer tuning of on-wafer measurements is intuitive and straightforward: Increasing the opening of the diffuser in any zone increases the plating rate relative to the other zones.

■ **Shielding**
Shielding affects only the outer ~10 mm of film thickness. If the film is seen to rise or drop suddenly around the edge of the wafer, shielding likely needs adjustment. If starting from an established process and looking to optimize, make 1 or 2 mm adjustments to shield height according to the on-wafer results obtained:

- If the plated film gets thicker at the wafer edge, there is too little shielding. Bring the shield upward.
- If the plated film gets thinner at the wafer edge, there is too much shielding. Lower the shield.
- If starting from the very beginning, it is recommended to set shield height to 6mm as measured from the out side of the shield.

Dialing In Cross-wafer Uniformity on a Non-ClassOne Plating System (and if there is no vendor-supplied POR Document)

1. Confirm the capabilities of your system:

■ **Control of fluid motion relative to wafer**

- Most newer systems are designed to enable spinning of the wafer during plating.
- Static wafer systems: Some systems have an archi tectures that fundamentally prohibit spinning of the wafer. Note that if the wafer cannot spin during plating, there will be fundamental limitations on achieving low uniformity numbers. Often, the best uniformity in such systems is achieved by slowing the plating rate.

■ **Electric field profile manipulation – available or not**

- Some systems provide no tuning for the electric field, which limits their capabilities.
- Systems providing for field tuning fall into one of two groups:
  - ◆ Tuning via physical diffuser. Typically this is a single, non-adjustable part.
  - ◆ Tuning using multiple, independently-controllable anodes. Multiple-anode systems add complexity (and cost) without measurable added value for a majority of plating applications. Most processes other than the latest-generation memory or logic devices can be readily tuned to excellent unifor mity by physical diffuser systems.

2. Set up your system for cross-wafer uniformity:

■ **Immersion**
Ensure that the wafer is fully and properly immersed in plating chemistry when in plating position. Note that some systems immerse the wafer truly horizontally, without the ability to tilt during wetting. This can trap air against the wafer and lead to non-uniform plating. Such systems usually require ramping the flow high and low repeatedly to evacuate bubbles. If your system does support tilt during wetting, then empirical testing should be done to confirm bubble-free immersion. If the system does not support

tilt during immersion but does support wafer spinning, ramping the wafer spin speed up and down may evacuate bubbles.

■ **Flow rate of chemistry**

Ideally, you will have a record of a "best known" flow rate for your system; if you don't, follow these guidelines:

- For gold plating: spin the wafer slowly (35-50 rpm) and use the higher end of flow rate for the system. This recommendation has more to do with Within-Fea ture Uniformity (addressed in the third part of this series), but the parameter should be set now.
- For most other metals: spin the wafer relatively fast (~100 rpm) and use a moderate flow rate.
- For static wafer systems: Flow rate is the only input that can be manipulated. Generally, higher is better.

■ **Plate a blanket seed wafer and make adjustments**

- Look at the profile of the plated film, compare it with the images provided above and make the sug gested changes.
- If you observe a rapid increase or rapid decrease of thickness at ~10mm from the edge, do the following:
  - ◆ A rapid increase in thickness is likely caused by too little shielding to offset current crowding. If your system has a 'shield' feature around the perimeter of the reactor, adjust it closer to the wafer. If the shield is not adjustable, you may need to adjust the plating position to be closer to the shield. If you have neither adjustment, there are few options to reduce this effect.
  - ◆ A rapid decrease in the outer 10mm of the wafer could have one of two causes: 1) Trapped bubbles from immersion. To correct this, see the suggestions above. 2) Too much shielding for offsetting the current crowding. To correct this, adjust the shield away from the wafer or the wafer away from the shield. If neither adjustment is available, this issue is not readily correctable.
- If center of profile is thick and "dome-like":
  - ◆ If field adjustment is possible, lower current density in the center
  - ◆ If field adjustment is not possible, increase spin speed by ~20rpm.
- If center of profile is thin:
  - ◆ If field adjustment is possible, lower current density around the edge of the wafer.
  - ◆ If field adjustment is not possible, decrease spin speed.
- The above adjustments can be repeated until the end result is within the desired specification.

Closing

We hope that this paper will be helpful to you in optimizing cross-wafer uniformity and product quality in your fab's electroplating processes. If you have additional questions about any of the above, please contact us at https://classone.com/inquire/. Our technology and applications teams have decades of semiconductor experience and a wealth of plating process knowledge, which we would be happy to share with you.

Please also see the other three parts of this Electroplating Fundamentals series which you can download from the ClassOne website at https://classone.com/tech-papers/.

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