Advanced Semiconductor Plating – Key Fundamentals

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Introduction

In semiconductor processing, each of the hundreds, millions, even billions of individual features on a given product wafer must meet tight specifications in order to achieve the product quality and yields required in today's fabs. Literally, every individual feature must be engineered to near perfection.

In electrochemical deposition (ECD) processes, fabs must have the ability to produce well-formed features that are not only void-free but also of perfect dimension; and all of this must be accomplished within an acceptable total system cost and operating cost.

ClassOne has developed this *Advanced Semiconductor Plating Series* to provide theory and practice guidance for today's electroplating engineers and operators to help them optimize their processes. Because of the broad scope of the topic, this series is arranged in four parts, as follows:

Part 1: Key Fundamentals and How to Dial In Target Plated Thickness

Part 2: Factors Affecting Localized Plating Rates and How to Optimize Cross-wafer Uniformity

Part 3: Wafer and Feature Effects and How to Optimize Feature Uniformity

Part 4: System-level Factors and How to Establish Repeatable Plating Performance

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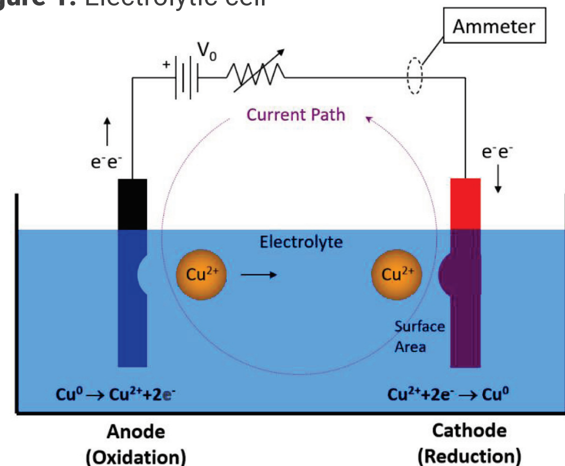
Individual Wafer in an Electrolytic Cell

A fundamental understanding of the basic electrolytic cell provides a valuable baseline from which to more deeply explore the specialized plating applications in the semiconductor industry. The most advanced plating applications for semiconductor manufacturing are based on the same principles as a standard, electrolytic cell. Figure 1 depicts an electrolytic cell with the following functional components: positive and negative electrodes, electrolyte, and power supply. In the specific example used, copper electrodes are immersed in a single copper sulfate-based electrolyte and connected to a power supply.

A potential is applied to the electrodes completing a circuit comprised of 1) electrons migrating through the wires

Figure 1. Electrolytic cell



that connect the electrodes and power supply and 2) the resultant electrolytic oxidation and reduction reactions at the electrodes and the ion flux through the electrolyte. The power supply provides electrons to the cathode where reduction reactions lead to the formation of copper metal. Transfer of electrons out of the cell at the anode results in oxidation reactions that release copper ions into solution, replenishing those consumed in formation of copper metal at the cathode.

As stated above, a voltage is applied to the cell and, because the circuit is complete, a current results [1]. This notion, that current is an output and not an input, is an important distinction because in most applications, a constant- or controlled-current process is desirable. To achieve this control, the current must be accurately read by an inline ammeter, with feedback to a controller, such that voltage can be modulated to keep output current on target.

$$I = V/R \qquad [1]$$

Where:
I = Current
V = Voltage
R = Resistance

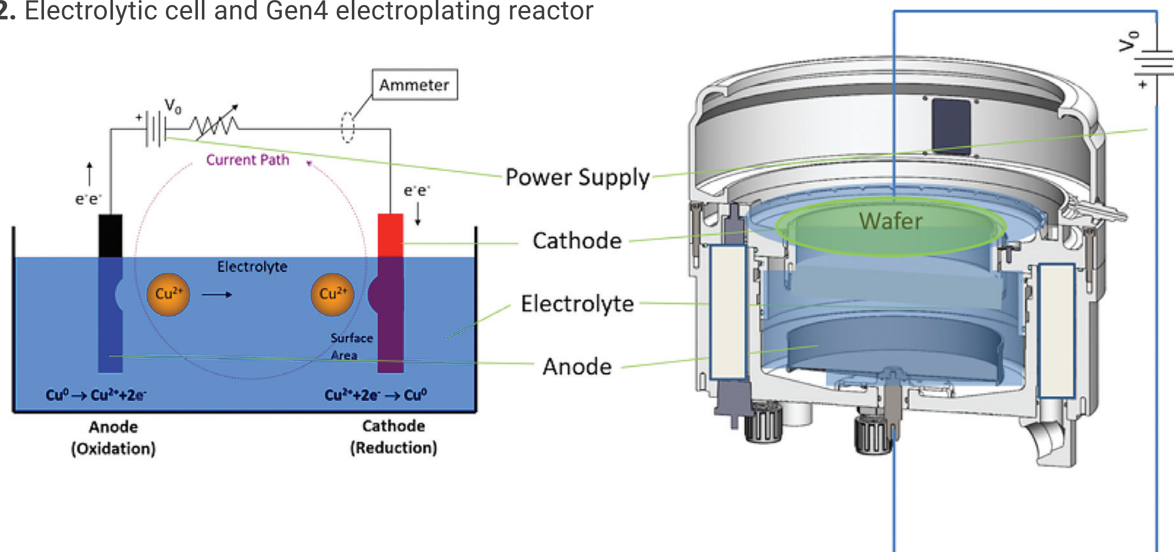
The Modern Semiconductor Plating Reactor

The basic electrolytic cell is indeed the foundation for all semiconductor plating reactors, including the reactors used to produce the most advanced plated features. While there are multiple types of reactors in use in the semiconductor industry, the specifications for leading products and devices drives the use of a single-wafer fountain reactor. All the major semiconductor manufacturers rely on some version of a face-down, single-wafer, fountain plating design. ClassOne Technology's Gen4 Reactor serves as a good example for uniformity discussions within this paper.

Each of the basic components from Figure 1 are present in the Gen4 Reactor, as shown in Figure 2. This document will focus on the basic design elements of a semiconductor reactor, but Part 2 of this series will highlight the uniformity requirements that drive the more specific design elements of such a reactor.

Whereas the illustration used in Figure 1 depicts electrodes vertically oriented, the Gen4 reactor places the anode in the bottom of the cell, with a horizontal orientation. This is to support efficient interaction with the cathode, which in semiconductor processing is the wafer itself. The wafer is also oriented horizontally, above the anode, with the plated surface facing down. There are distinct advantages to this configuration as will be discussed in this paper. Continuing with copper as the metallization example for this discussion, it is most common that the anode be composed of copper[1]

Figure 2. Electrolytic cell and Gen4 electroplating reactor



[1] In fact, in semiconductor copper plating, it is most common to use copper anode material that contains trace amounts of phosphorus.

and that the anode be consumed over time as part of the reaction, though this paper will later discuss applications where an inert anode is used.

Plating electrolytes in semiconductor applications are highly specialized, as will be covered later, but in the case of copper, the electrolyte remains a copper sulfate-based solution.

The anode and wafer are connected electrically, through hardware and wiring, to a power supply. In the case of the semiconductor reactor, the power supply is rather sophisticated in its control capability. The power supply of a state-of-the-art plating tool will include capability for highly precise current control, which is critical in meeting the uniformity requirements of the industry.

Relating Electrical Current to Plated Feature Dimensions

It is important to note that deposition of high-quality plated films requires that the system operate in an electron deficient condition. In other words, the voltage is controlled such that the current restricts the rate of reaction. This ensures that electron supply serves as a limiting reagent in the reduction reactions at the wafer surface. The electron-poor condition provides two key benefits to the plating process:

- Avoids encroaching on the Limiting Current Density for the specific application, which, when encountered, produces deposits of poor quality (covered in detail in Part 2 of this series).
- Provides very accurate control of reaction rate and thus deposition rate since current is very precisely controlled.

The current delivered to a wafer produces plated material according to the specific electrochemical reactions for the given process. In the case of the basic copper plating example used here, the fundamental cathodic reaction that produces plated copper is[2]:

$$Cu^{2+} + 2e^{-} \rightarrow Cu^{0} \quad [2]$$

Where:

- Cu^{2+} is the cupric ion in the copper deposition
- e^{-} is the electron supplied by the power supply
- Cu^{0} is the solid copper deposited

While there are reaction efficiencies to be considered, one can quickly discern that the number moles of electrons produced will result in a proportionate number of moles of solid copper deposited. It follows that a given number of moles of electrons will produce a specific mass of plated copper.

Because the density of the deposited copper is constant, this mass of copper has a certain volume. Thus, the volume of copper plated to a wafer is directly proportional to the number of moles of electrons provided to the system[3]. This means that a modern plating system like Solstice can produce a very precise volume of metal on the wafer by controlling the total current applied.

Physical volume is expressible as width x length x height. The horizontal dimensions of the feature are controlled by the wafer itself. In the case of features plated within a patterned mask, the horizontal dimensions of the feature are tightly defined by the patterning of the lithography steps. This incoming area is referred to as open area since it is available for plating. This leads to consideration of plating height or thickness.

Because the applied current encounters a controlled area, the given current is distributed across this area, meaning that the discussion of current really is a discussion of current over area, in other words, current density (J) typically stated in units of milliamps per square centimeter (mA/cm^2) or amps per square decimeter (ASD). This paper will hereafter provide examples strictly in terms of mA/cm^2.[4]

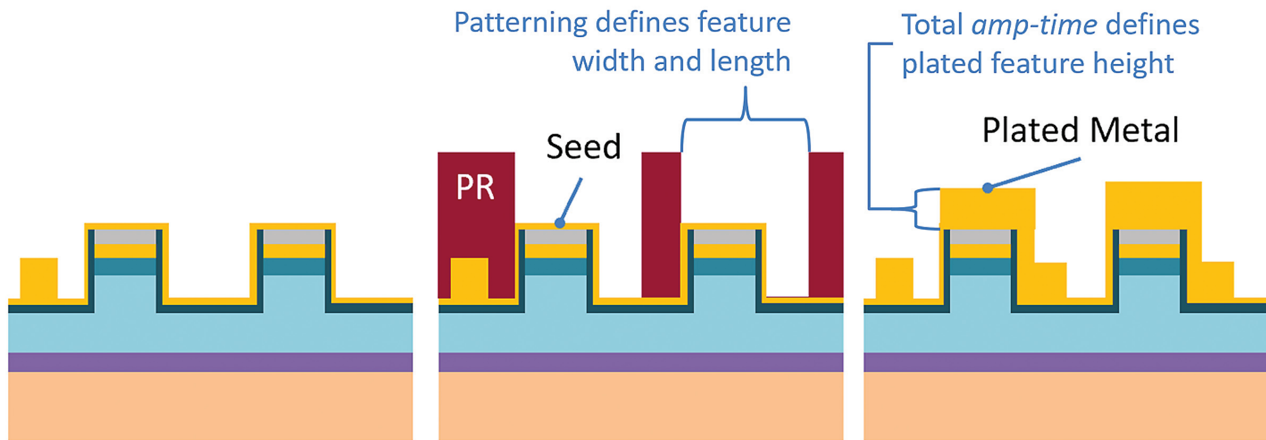
Putting this together, current density drives plating rate. In more practical terms as regards the formation of electrical features, which is the purpose of plating in the semiconductor industry, and particularly in the case of features plated within a patterned mask, current density drives the rate of vertical growth of the plated material forming the feature. Put another way, the current density applied in a given

[2] In actuality, there are many more reactions involved in copper deposition, especially in the case of superconformal copper filling. However, such detail is beyond the scope of this work.

[3] Recall that an ampere is actually a unit expressing a rate: 1 ampere = 1 Coulomb/second.

[4] As a reference, $10mA/cm^2$ = 1ASD.

Figure 3. Device cross-section illustration – relationship between charge and plated feature height



system, is readily converted to a thickness-per-time term, most often in units of micrometers per minute (μm/min).

The discussion to this point has accounted for the rate of deposition. Controlling the final plated height then requires control of the duration of plating. This can be accomplished by performing the plating step to a set time. But there is an additional control option that provides even greater accuracy, and that is to control the total charge delivered.

Terminating the plating step according to step time assumes the current holds perfectly to target and also relies greatly on the precision of the system's timing functions. However, a more accurate mode of plating height control is achieved by terminating the plating step when a certain charge is reached. If charge is stated in units of amp-hours, it becomes obvious how current density applied for a certain time results in a specific thickness. Charge-based step termination takes advantage of the precise current control of modern semiconductor power supplies.

In summary:

- Electron supply ➔ rate of reaction at wafer ➔ rate of metal deposition
- Total charge (amp-hour) ➔ height of deposited metal for a defined plated area

Plating the First Wafer: How to Achieve Target Plated Thickness

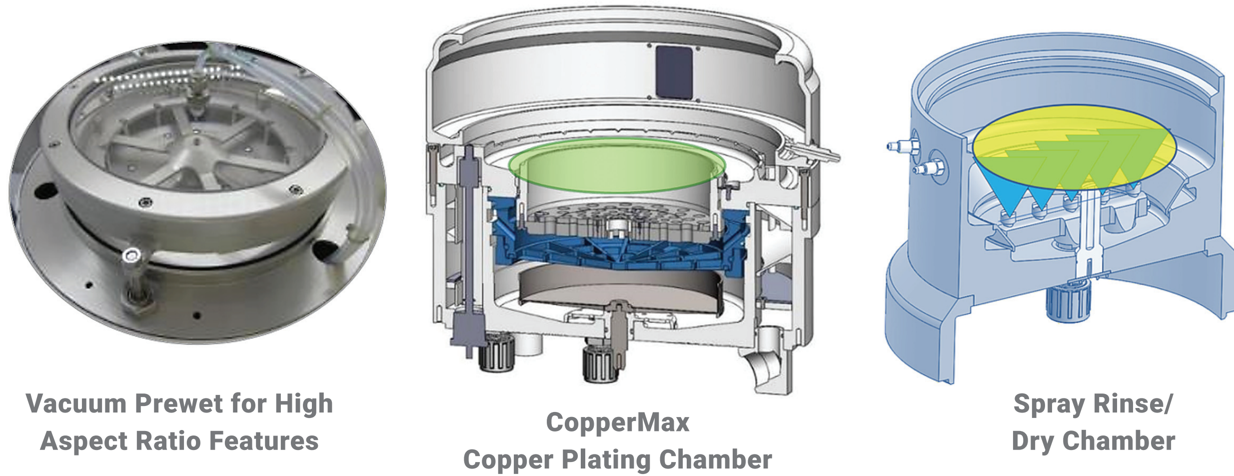
This section describes in brief how to dial in a plating process to achieve the target feature height or thickness. Of course, there are additional considerations beyond the scope of this document. For this reason, some clarifications and a statement of assumptions are in order.

Process sequence: It is best if the reader of this work has a known functional starting sequence. If the system in use is new or the user of the plating system is new to it, then some time will need to be spent in establishing a functioning starting point, whereby the system is being operated as designed.

If the system in use is a ClassOne Technology Solstice system, the ClassOne Technology Process of Record (POR) document will provide a clear definition. If the system in use is a Solstice and a POR document is not available, please contact the Applications Group at c1tdc@classone.com and request one.

Please note that there are many highly specialized plating applications, so there is no single guaranteed solution for every possible case. However, ClassOne's experience can help move the application forward quickly. If the system in use is not a Solstice and the starting point is not well established, ClassOne's application team can still give guidance on a starting point.

Figure 4. Examples of ClassOne process chambers for a vacuum prewet ➔ plating ➔ rinse dry sequence



The following are recommended steps to dialing in target plated height/thickness:

1. Identify the starting sequence. The baseline example that will be used here is given below (note that this may vary based on application):

Plasma Pretreatment ➔ Prewet ➔ Plating ➔ Rinse dry

Regarding the plasma pretreatment or descum step, ClassOne recommends this in all cases unless either: the sequence is already known and demonstrated not to need it, or the use of an oxygen plasma step would be detrimental in some way to the wafer or substrate.

The purpose of including a plasma pretreatment is to create a readily wettable surface. Wettability is important on wafers and substrates patterned with photoresist; but the step is also valuable on wafers with no photoresist present, since organic monolayers are readily formed even in the cleanest of fabs.

Regarding the prewet step, many plating applications do not require a prewet of any kind, and yet others cannot be reliably completed without it. Questions on this topic may be addressed to ClassOne's Technology Development Center at c1tdc@classone.com.

Basic guidance is this:

- If the established sequence already includes a prewet, retain it for the purposes of dialing in plated thickness. A separate test plan should be used if the interest is to eliminate a prewet.
- If there is no established sequence:
  - Wafers with no photoresist patterning and with feature aspect ratios lower than 3:1 typically do not need prewet
  - Wafers with feature aspect ratios higher than 3:1 or with photoresist patterning benefit from a deionized water (DI) spray prewet.
  - Wafers with feature aspect ratio higher than 5:1 may benefit most from a vacuum prewet step.

2. Collect all pertinent input information in anticipation of the calculations necessary. For convenience, ClassOne has simplified the many equations involving stoichiometric ratios, valence numbers, etc. down to the following:

Open Area: $$OA = O * ((D/20) - (EE/10))^2 * \pi \quad [3]$$

Current Setpoint: $$I = OA * J/1000 \quad [4]$$

Charge (for Step Termination)**:** $$Q = f_Q * T * OA \quad [5]$$

Plating Time: $$t = Q / I \quad [6]$$

Efficiency Calculation: $$E = \Delta m * fE / Q \quad [7]$$

Where:

- OA = Open Area of the wafer in units of cm^2; i.e., the area of seed metal exposed where plating will occur.
- T = Target Plated Film Thickness, in μm, for a given metal, i.e., plated height.
- t = Plating Time necessary to achieve target plated film thickness.
- O = Fraction of Open Area. In other words, this is the fraction of the wafer surface that is NOT covered by photoresist. Often, with TWV, there is no photoresist present and this value is 1 (representing 100%).
- D = Diameter of the wafer in mm.
- EE = Edge Exclusion Width in mm, also understood as the width of wafer edge where plating will not occur. If the plating system in use employs a plating seal to minimize maintenance, as Solstice does, then the EE is the distance that the seal reaches in from the edge of the wafer. If the plating system does not include a seal, this number is likely defined by how far in from wafer edge the seed begins. If the seed coverage extends to the very edge of the wafer, then this value is 0.
- J = Current Density in mA/cm^2. This value is best determined from the chemistry manufacturer's Technical Data Sheet (TDS) or from the previously established POR.
- f_Q = Charge Factor. This is an empirically derived factor to simplify estimation of charge value. Values for each plated metal are found in Table 1.
- I = Current in Amperes. Value entered into the recipe for current setpoint. In the Solstice recipe editor, this value is expressed as *PPS Fwd Curr*. Confirm the unit used in the specific plating system, in case a different unit is used, e.g., milliamps.
- Q = Charge in Amp-Minutes. Solstice provides a recipe input for this value to serve as step termination. If the system being used does the same then this value can be used to accurately end the step. Confirm the units for input into the plating system control/recipe. In the Solstice recipe editor, this value is expressed as *PPS Amp Min* and the input units are amp-minutes.
- E = Plating Efficiency (aka *cathode efficiency*).
- Δm = Measured Change in Wafer Mass due to plating.
- f_E = Plating Efficiency Factor. This is an empirically derived factor to simplify estimation of plating efficiency. Values for each plated metal are found in Table 1.

Table 1. Charge and Efficiency Factors

Plated Film	f_Q	f_E
Au	0.0158	32.63
Cu	0.0441	198.2
In	0.0307	56.01
Ni	0.0471	105.7
Sn	0.0200	108.3

3. ClassOne recommends weighing the wafer before plating. This allows for estimations of plating efficiency. The scale should have measurement resolution to 0.0005g.

4. Perform the calculation in equation [3] to determine open area, if it is not otherwise known.

5. Perform the calculation in equation [4] to determine the correct current setpoint necessary to achieve the intended current density.

6. Determine whether the recipe will terminate plating based on time or charge and perform the associated calculation; either [5] or [6].

7. Enter the current setpoint and step termination value into the recipe.

8. Plate the wafer according to the defined sequence.

9. Measure the mass again as a quick confirmation of plating efficiency. Perform calculation [7] to establish the efficiency value. The chemistry vendor's TDS should provide an expected efficiency range for chemistry in use.

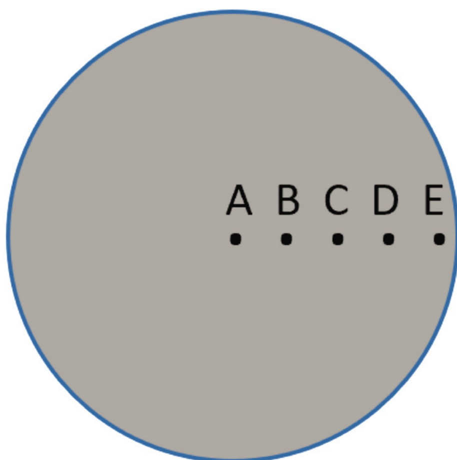
10. Measure feature height and compare against expected. For wafers with a patterned photoresist, it is best to strip the resist for accurate feature height measurement. Because this work has not covered dialing in of uniformity, ClassOne recommends measuring the wafer at multiple locations and taking an average for evaluating the actual against target.

Recommended measurement locations for different wafer diameters are shown in Table 2 and Figure 4.

Table 2. Suggested Measurement Points for Determining Plated Thickness

Wafer Diameter	Distance from Wafer Center (mm)				
	A	B	C	D	E
75	0	8	16	24	32
100	0	12	25	35	45
150	0	17	35	52	70
200	0	22	45	72	95
300	0	35	70	100	145

Figure 4. Suggested Measurement Map



11. Assuming there are no genuine faults within the systems in use, the resultant plated height should be close to target and only minor adjustments should be necessary to get directly on target. Make the adjustments to plating time or total charge and repeat the steps, and within two or three attempts the target plated height/thickness should be achieved.

Closing

This document has presented a combination of fundamental principles and practical instructions on semiconductor electroplating. The goal is to enable engineers and equipment operators to more clearly understand their plating applications and more efficiently dial in the plating sequence to achieve desired plated thicknesses.

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Mr. Carter is a product and process development engineer of electrochemical systems including semiconductor plating and advanced battery manufacturing. He is co-inventor on multiple patents enabling electrochemical systems. At ClassOne, Mr. Carter is responsible for driving process hardware development for the advancement of plating and surface preparation applications. He is a graduate of the Katholieke Universiteit Leuven.

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